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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT573

Octal D-type transparent latch; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

# Octal D-type transparent latch; 3-state 74HC/HCT573

## FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the “563” and “373”
- Output capability: bus driver
- $I_{CC}$ category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.
A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The “573” consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the $D_n$ inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.
When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state.
Operation of the $\overline{OE}$ input does not affect the state of the latches.

The “573” is functionally identical to the “563” and “373”, but the “563” has inverted outputs and the “373” has a different pin arrangement.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f$ = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | HC | HCT | |
| $t_{PHL}/ t_{PLH}$ | propagation delay | $C_L$ = 15 pF; $V_{CC}$ = 5 V | | | |
| | $D_n$ to $Q_n$ | | 14 | 17 | ns |
| | LE to $Q_n$ | | 15 | 15 | ns |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per latch | notes 1 and 2 | 26 | 26 | pF |

### Notes

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   $C_L$ = output load capacitance in pF; $V_{CC}$ = supply voltage in V
2. For HC the condition is $V_I$ = GND to $V_{CC}$; for HCT the condition is $V_I$ = GND to $V_{CC}$ – 1.5 V

## ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

**PIN DESCRIPTION**

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 2, 3, 4, 5, 6, 7, 8, 9 | $D_0$ to $D_7$ | data inputs |
| 11 | LE | latch enable input (active HIGH) |
| 1 | $\overline{OE}$ | 3-state output enable input (active LOW) |
| 10 | GND | ground (0 V) |
| 19, 18, 17, 16, 15, 14, 13, 12 | $Q_0$ to $Q_7$ | 3-state latch outputs |
| 20 | $V_{CC}$ | positive supply voltage |

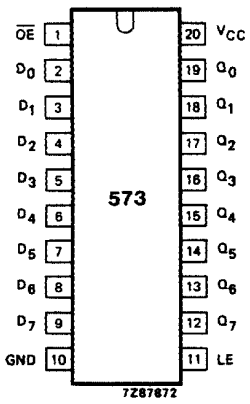



Fig.1 Pin configuration.

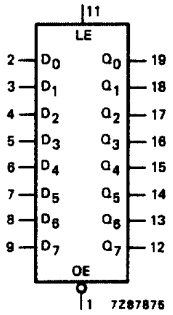



Fig.2 Logic symbol.

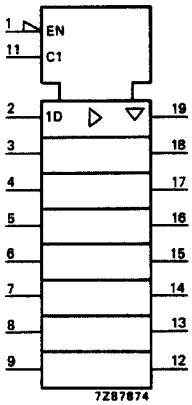



Fig.3 IEC logic symbol.

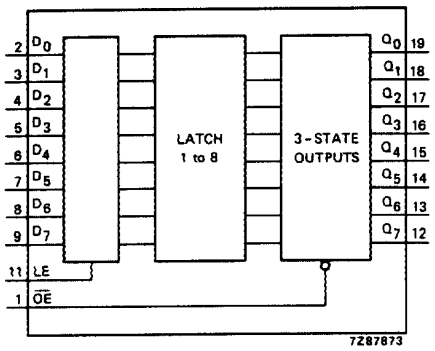



Fig.4 Functional diagram.

**FUNCTION TABLE**

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS |
|---|---|---|---|---|---|
| | $\overline{OE}$ | LE | $D_N$ | | $Q_0$ to $Q_7$ |
| enable and read register (transparent mode) | L<br>L | H<br>H | L<br>H | L<br>H | L<br>H |
| latch and read register | L<br>L | L<br>L | l<br>h | L<br>H | L<br>H |
| latch register and disable outputs | H<br>H | L<br>L | l<br>h | L<br>H | Z<br>Z |

**Notes**

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
   Z = high impedance OFF-state

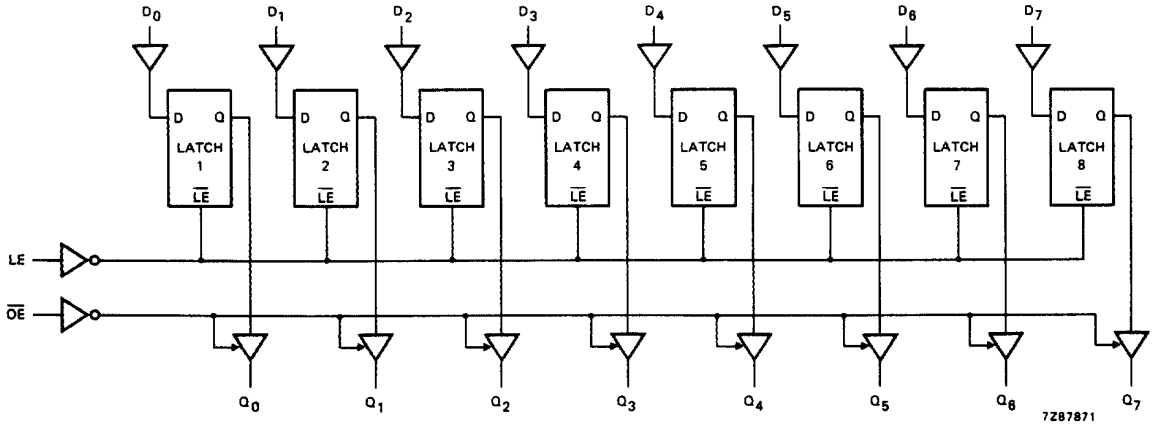



Fig.5 Logic diagram.

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
$I_{CC}$ category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HC | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | –40 to +85 | | –40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay $D_n$ to $Q_n$ | | 47<br>17<br>14 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_{PHL}$/ $t_{PLH}$ | propagation delay LE to $Q_n$ | | 50<br>18<br>14 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{PZH}$/ $t_{PZL}$ | 3-state output enable time $\overline{OE}$ to $Q_n$ | | 44<br>16<br>13 | 140<br>28<br>24 | | 175<br>35<br>30 | | 210<br>42<br>36 | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{PHZ}$/ $t_{PLZ}$ | 3-state output disable time $\overline{OE}$ to $Q_n$ | | 55<br>20<br>16 | 150<br>30<br>26 | | 190<br>38<br>33 | | 225<br>45<br>38 | ns | 2.0<br>4.5<br>6.0 | Fig.8 |
| $t_{THL}$/ $t_{TLH}$ | output transition time | | 14<br>5<br>4 | 60<br>12<br>10 | | 75<br>15<br>13 | | 90<br>18<br>15 | ns | 2.0<br>4.5<br>6.0 | Fig.6 |
| $t_W$ | enable pulse width HIGH | 80<br>16<br>14 | 14<br>5<br>4 | | 100<br>20<br>17 | | 120<br>24<br>20 | | ns | 2.0<br>4.5<br>6.0 | Fig.7 |
| $t_{su}$ | set-up time $D_n$ to LE | 50<br>10<br>9 | 11<br>4<br>3 | | 65<br>13<br>11 | | 75<br>15<br>13 | | ns | 2.0<br>4.5<br>6.0 | Fig.9 |
| $t_h$ | hold time $D_n$ to LE | 5<br>5<br>5 | 3<br>1<br>1 | | 5<br>5<br>5 | | 5<br>5<br>5 | | ns | 2.0<br>4.5<br>6.0 | Fig.9 |

### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
$I_{CC}$ category: MSI

### Note to HCT types

The value of additional quiescent supply current ($\Delta I_{CC}$) for a unit load of 1 is given in the family specifications. To determine $\Delta I_{CC}$ per input, multiply this value by the unit load coefficient shown in the table below.

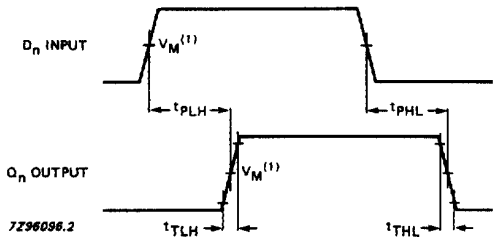
| INPUT | UNIT LOAD COEFFICIENT |
|---|---|
| $D_n$ | 0.35 |
| $\overline{LE}$ | 0.65 |
| $\overline{OE}$ | 1.25 |

### AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; $C_L$ = 50 pF

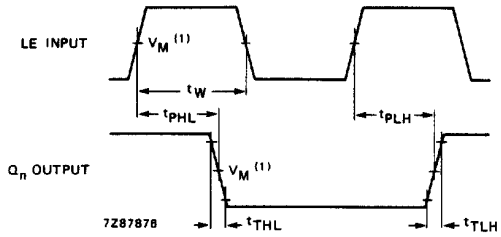
| SYMBOL | PARAMETER | $T_{amb}$ (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 74HCT | | | | | | | | $V_{CC}$ (V) | WAVEFORMS |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| $t_{PHL}/ t_{PLH}$ | propagation delay $D_n$ to $Q_n$ | | 20 | 35 | | 44 | | 53 | ns | 4.5 | Fig.6 |
| $t_{PHL}/ t_{PLH}$ | propagation delay LE to $Q_n$ | | 18 | 35 | | 44 | | 53 | ns | 4.5 | Fig.7 |
| $t_{PZH}/ t_{PZL}$ | 3-state output enable time $\overline{OE}$ to $Q_n$ | | 17 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 |
| $t_{PHZ}/ t_{PLZ}$ | 3-state output disable time $\overline{OE}$ to $Q_n$ | | 18 | 30 | | 38 | | 45 | ns | 4.5 | Fig.8 |
| $t_{THL}/ t_{TLH}$ | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.6 |
| $t_W$ | enable pulse width HIGH | 16 | 5 | | 20 | | 24 | | ns | 4.5 | Fig.7 |
| $t_{su}$ | set-up time $D_n$ to LE | 13 | 7 | | 16 | | 20 | | ns | 4.5 | Fig.9 |
| $t_h$ | hold time $D_n$ to LE | 9 | 4 | | 11 | | 14 | | ns | 4.5 | Fig.9 |

## AC WAVEFORMS



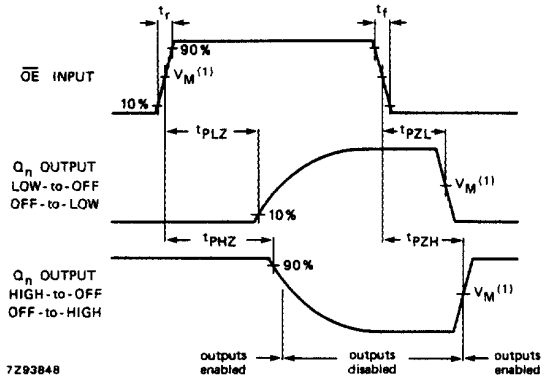

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.6 Waveforms showing the data input ($D_n$) to output ($Q_n$) propagation delays and the output transition times.



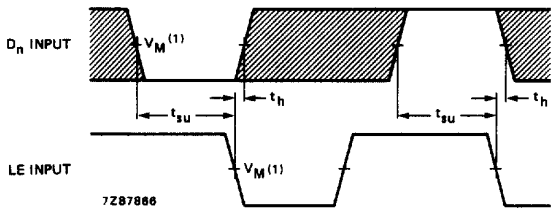

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output ($Q_n$) propagation delays and the output transition times.




(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.8 Waveforms showing the 3-state enable and disable times.




The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
HCT: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.9 Waveforms showing the data set-up and hold times for $D_n$ input to LE input.

## PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.