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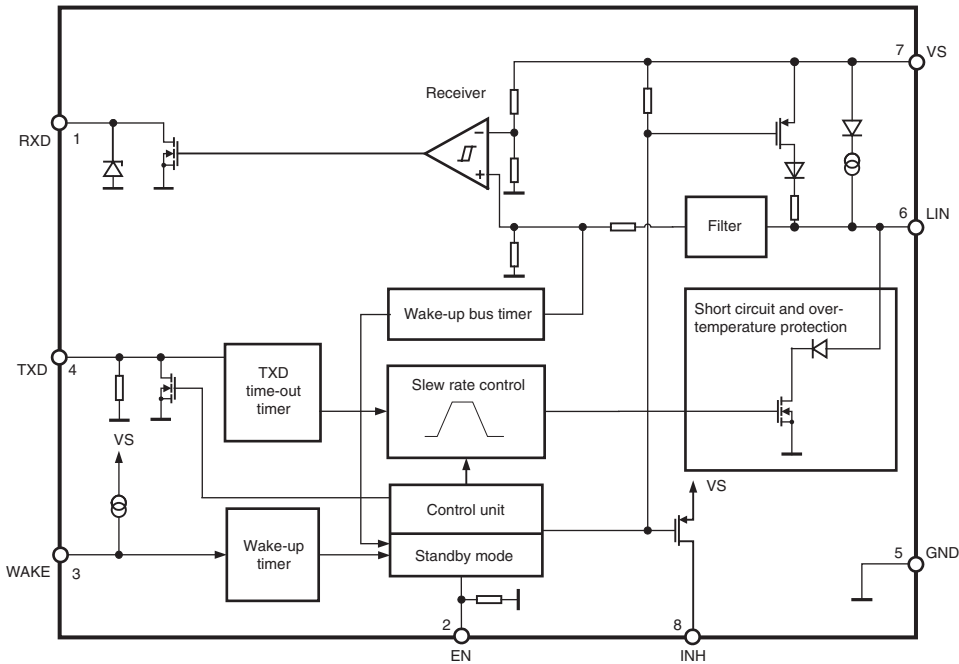
Features

- Operating Range from 5V to 27V
- Baud Rate up to 20 Kbaud
- Improved Slew Rate Control According to LIN Specification 2.0 and SAEJ2602-2
- Fully Compatible with 3.3V and 5V Devices
- Dominant Time-out Function at Transmit Data (TXD)
- Normal and Sleep Mode
- Wake-up Capability via LIN Bus (90 μ s Dominant)
- External Wake-up via WAKE Pin (35 μ s Low Level)
- Control of External Voltage Regulator via INH Pin
- Very Low Standby Current During Sleep Mode (10 μ A)
- Wake-up Source Recognition
- Bus Pin Short-circuit Protected versus GND and Battery
- LIN Input Current Typically 5 μ A if V_{BAT} Is Disconnected
- Overtemperature Protection
- High EMC Level
- Interference and Damage Protection According to ISO/CD 7637
- ESD HBM 6 kV at LIN Bus Pin and Supply VS Pin

1. Description

The ATA6662 is a fully integrated LIN transceiver complying with the LIN specification 2.0 and SAEJ2602-2. It interfaces the LIN protocol handler and the physical layer. The device is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN bus ensures secure data communication up to 20 Kbaud with an RC oscillator for protocol handling. Sleep mode guarantees minimal current consumption. The ATA6662 has advanced EMI and ESD performance.

Figure 1-1. Block Diagram



LIN Transceiver

ATA6662

Preliminary



2. Pin Configuration

Figure 2-1. Pinning SO8

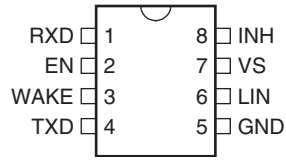


Table 2-1. Pin Description

Pin	Symbol	Function
1	RXD	Receive data output (open drain)
2	EN	Enables normal mode; when the input is open or low, the device is in sleep mode
3	WAKE	High voltage input for local wake-up request
4	TXD	Transmit data input; active low output (strong pull-down) after a local wake-up request
5	GND	Ground, heat sink
6	LIN	LIN bus line input/output
7	VS	Battery supply
8	INH	Battery-related inhibit output for controlling an external voltage regulator; active high after a wake-up request

3. Functional Description

3.1 Supply Pin (V_S)

Undervoltage detection is implemented to disable transmission if V_S falls to a value below 5V in order to avoid false bus messages. After switching on V_S , the IC switches to pre-normal mode and INHIBIT is switched on. The supply current in sleep mode is typically 10 μ A.

3.2 Ground Pin (GND)

The ATA6662 is neutral on the LIN pin in the case of a GND disconnection. It is able to handle a ground shift up to 11.5% of V_S .

3.3 Bus Pin (LIN)

A low-side driver with internal current limitation and thermal shutdown and an internal pull-up resistor are implemented as specified for LIN 2.0. The voltage range is from $-27V$ to $+40V$. This pin exhibits no reverse current from the LIN bus to V_S , even in the case of a GND shift or V_{Batt} disconnection. The LIN receiver thresholds are compatible to the LIN protocol specification. The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled. The output has a self-adapting short circuit limitation; that is, during current limitation, as the chip temperature increases, the current is reduced.

3.4 Input Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD is low to bring LIN low. If TXD is high, the LIN output transistor is turned off. Then, the bus is in recessive mode via the internal pull-up resistor. The TXD pin is compatible to both a 3.3V or 5V supply.

3.5 TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced low longer than $t_{dom} > 6$ ms, the pin LIN will be switched off (recessive mode). To reset this mode, switch TXD to high (>10 μ s) before switching LIN to dominant again.

3.6 Output Pin (RXD)

This pin reports to the microcontroller the state of the LIN bus. LIN high (recessive) is reported by a high level at RXD, LIN low (dominant) is reported by a low voltage at RXD. The output is an open drain, therefore, it is compatible to a 3.3V or 5V power supply. The AC characteristics are defined with a pull-up resistor of 5 k Ω to 5V and a load capacitor of 20 pF. The output is short-current protected. In unpowered mode ($V_S = 0V$), RXD is switched off. For ESD protection a Zener diode is integrated, with $V_Z = 6.1V$.

3.7 Enable Input Pin (EN)

This pin controls the operation mode of the interface. If EN = 1, the interface is in normal mode, with the transmission path from TXD to LIN and from LIN to Rx both active. A falling edge on EN while TXD is already set to high, the device is switched to sleep mode and no transmission is possible. In sleep mode, the LIN bus pin is connected to V_S with a weak pull-up current source. The device can transmit only after being woken up (see [Section 3.8, “Inhibit Output Pin \(INH\)”](#)).

During sleep mode the device is still supplied from the battery voltage. The supply current is typically 10 μA . The pin EN provides a pull-down resistor in order to force the transceiver into sleep mode in case the pin is disconnected.

3.8 Inhibit Output Pin (INH)

This pin is used to control an external switchable voltage regulator having a wake-up input. The inhibit pin provides an internal switch towards pin V_S . If the device is in normal mode, the inhibit high-side switch is turned on and the external voltage regulator is activated. When the device is in sleep mode, the inhibit switch is turned off and disables the voltage regulator.

A wake-up event on the LIN bus or at pin WAKE will switch the INH pin to the V_S level. After a system power-up (V_S rises from zero), the pin INH switches automatically to the V_S level. The R_{DSon} of the high-side output is $< 1 \text{ k}\Omega$.

3.9 Wake-up Input Pin (WAKE)

This pin is a high-voltage input used to wake the device up from sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. If you do not need a local wake-up in your application, connect pin WAKE directly to pin VS. A pull-up current source with typically $-10 \mu\text{A}$ is implemented. The voltage threshold for a wake-up signal is 3V below the VS voltage with an output current of typically $-3 \mu\text{A}$.

Wake-up events from sleep mode:

- LIN bus
- EN pin
- WAKE pin

[Figure 3-1 on page 6](#), [Figure 3-2 on page 7](#) and [Figure 3-3 on page 7](#) show details of wake-up operations.

3.10 Operation Modes

1. Normal mode
This is the normal transmitting and receiving mode. All features are available.
2. Sleep mode
In this mode the transmission path is disabled and the device is in low power mode. Supply current from V_{Batt} is typically 10 μA . A wake-up signal from the LIN bus or via pin WAKE will be detected and will switch the device to pre-normal mode. If EN then switches to high, normal mode is activated. Input debounce timers at pin WAKE (T_{WAKE}), LIN (T_{BUS}) and EN (T_{sleep}, T_{nom}) prevent unwanted wake-up events due to automotive transients or EMI. In sleep mode the INH pin is left floating. The internal termination between pin LIN and pin V_S is disabled to minimize the power dissipation in case pin LIN is short-circuited to GND. Only a weak pull-up current (typical 10 μA) between pin LIN and pin V_S is present. The sleep mode can be activated independently from the actual level on pin LIN or WAKE, guaranteeing that the lowest power consumption is achievable even in the case of a continuous dominant level on pin LIN or a continuous LOW on pin WAKE.
3. Pre-normal mode
At system power-up, the device automatically switches to pre-normal mode. It switches the INH pin to a high state, to the V_S level. The microcontroller of the application will then confirm the normal mode by setting the EN pin to high.

3.11 Remote Wake-up via Dominant Bus State

A voltage less than the LIN pre-wake detection V_{LINL} at pin LIN activates the internal LIN transceiver.

A falling edge at pin LIN, followed by a dominant bus level V_{BUSdom} maintained for a certain time period (T_{BUS}) and a rising edge at pin LIN results in a remote wake-up request.

The device switches to pre-normal mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see [Figure 3-2 on page 7](#)).

3.12 Local Wake-up via Pin WAKE

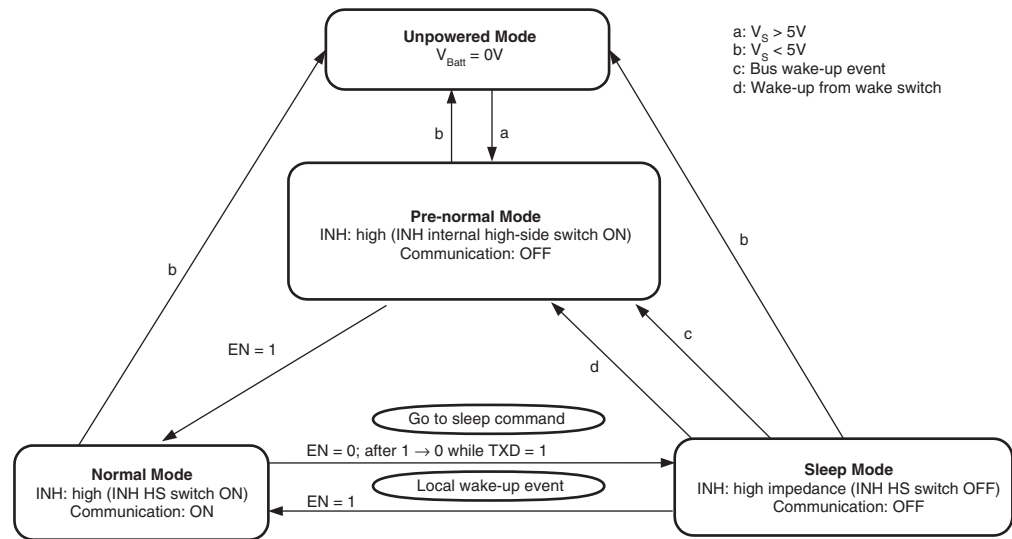
A falling edge at pin WAKE, followed by a low level maintained for a certain time period (T_{WAKE}), results in a local wake-up request. The wake-up time (T_{WAKE}) ensures that no transient, according to ISO7637, creates a wake-up. The device switches to pre-normal mode. Pin INH is activated (switches to V_S) and the internal termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller and a strong pull-down at pin TXD (see [Figure 3-3 on page 7](#)). The voltage threshold for a wake-up signal is 3V below the V_S voltage with an output current of typical $-3 \mu A$. Even in the case of a continuous low at pin WAKE it is possible to switch the IC into sleep mode via a low at pin EN. The IC will stay in sleep mode for an unlimited time. To generate a new wake up at pin WAKE it needs first a high signal $> 6 \mu s$ before a negative edge starts the wake-up filtering time again.

3.13 Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (dominant LIN bus). The wake-up source can be read on pin TXD in pre-normal mode. If an external pull-up resistor (typically 5 k Ω) has been added on pin TXD to the power supply of the microcontroller, a high level indicates a remote wake-up request (weak pull-down at pin TXD) and a low level indicates a local wake-up request (strong pull-down at pin TXD).

The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately if the microcontroller sets pin EN to high (see [Figure 3-2 on page 7](#) and [Figure 3-3 on page 7](#)).

Figure 3-1. Mode of Operation



3.14 Fail-safe Features

- There are now reverse currents $< 15 \mu A$ at pin LIN during loss of V_{BAT} or GND; this is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.
- Pin EN provides a pull-down resistor to force the transceiver into sleep mode if EN is disconnected.
- Pin RXD is set floating if V_{BAT} is disconnected.
- Pin TXD provides a pull-down resistor to provide a static low if TXD is disconnected.
- The LIN output driver has a current limitation, and if the junction temperature T_j exceeds the thermal shut-down temperature T_{off} , the output driver switches off.
- The implemented hysteresis, T_{hys} , enables the LIN output again after the temperature has been decreased.

Figure 3-2. LIN Wake-up Waveform Diagram

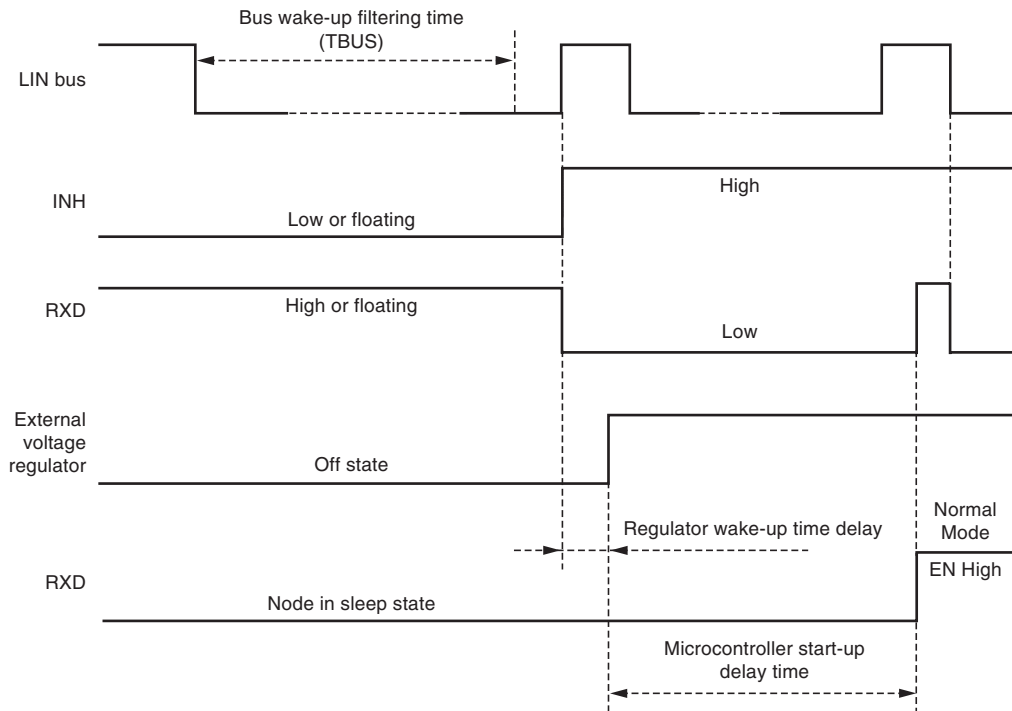
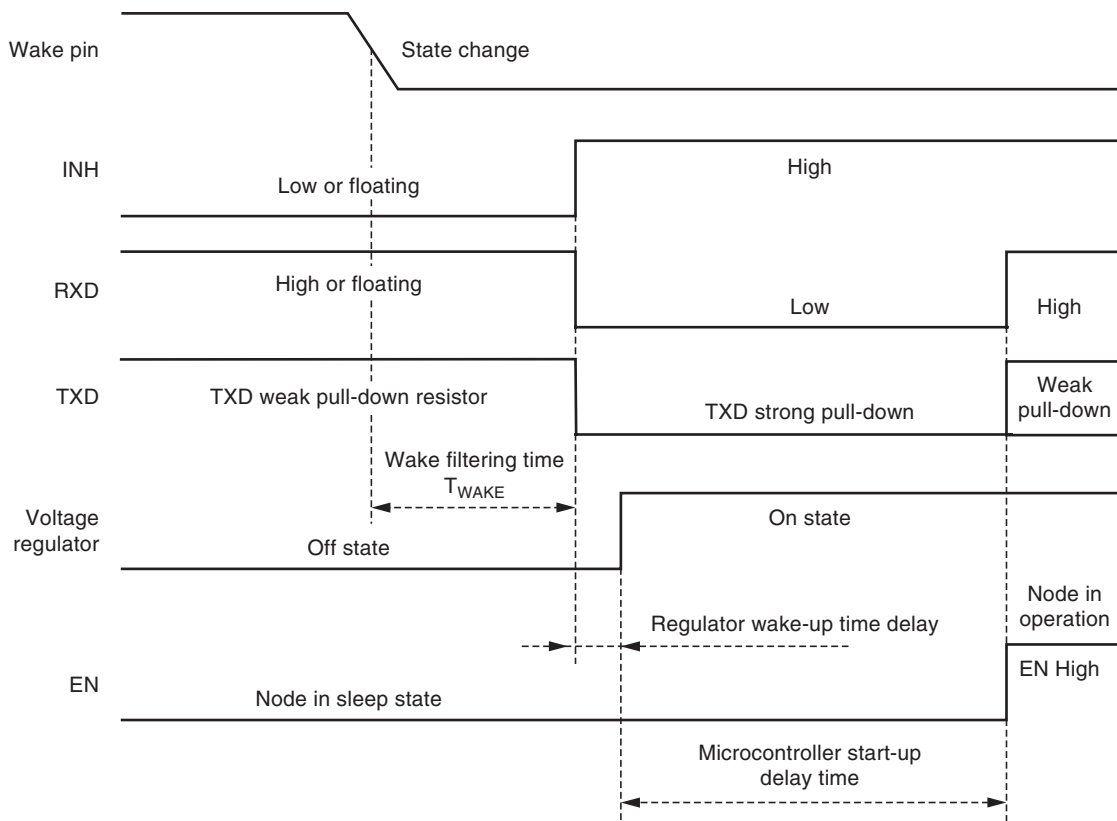


Figure 3-3. Wake-up from Wake-up Switch



4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Typ.	Max.	Unit
V_S - Continuous supply voltage		-0.3		+40	V
Wake DC and transient voltage (with 33-k Ω serial resistor) - Transient voltage due to ISO7637 (coupling 1 nF)		-1 -150		+40 +100	V V
Logic pins (RXD, TXD, EN)		-0.3		+5.5	V
LIN - DC voltage - Transient voltage due to ISO7637 (coupling 1 nF)		-27 -150		+40 +100	V V
INH - DC voltage		-0.3		+40	V
According to IBEE LIN EMC Test specification 1.0 following IEC 61000-4-2 - Pin VS, LIN to GND - Pin WAKE (33 k Ω serial resistor)		± 6 ± 5			KV KV
ESD HBM following STM5.1 with 1.5 k Ω /100 pF - Pin VS, LIN, WAKE to GND - Pin INH to GND		± 8 ± 6			KV KV
HBM ESD ANSI/ESD-STM5.1 JESD22-A114 AEC-Q100 (002)		± 3			KV
CDM ESD STM 5.3.1		± 750			V
Junction temperature	T_j	-40		+150	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55		+150	$^{\circ}\text{C}$
Thermal shutdown	T_{off}	150	165	180	$^{\circ}\text{C}$
Thermal shutdown hysteresis	T_{hys}	5	10	20	$^{\circ}\text{C}$

Note: 1. Equivalent to discharge a 100-pF capacitor through a 1.5-k Ω resistor.

5. Thermal Resistance

Parameters	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance junction ambient	R_{thJA}			145	K/W
Special heat sink at GND (pin 5) on PCB (fused lead frame to pin 5)	R_{thJA}		80		K/W

6. Electrical Characteristics

5V < V_S < 27V, T_J = -40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	V_S Pin								
1.1	DC voltage range nominal		7	V _S	5	13.5	27	V	A
1.2	Supply current in sleep mode	Sleep mode V _{lin} > V _{Batt} - 0.5V V _{Batt} < 14V	7	I _{V_Ssstby}		10	20	μA	A
1.3	Supply current in normal mode	Bus recessive	7	I _{V_Srec}		1.6	3	mA	A
1.4		Bus dominant Total bus load > 500Ω	7	I _{V_Sdom}		1.6	3	mA	A
1.5	V _S undervoltage threshold			V _{Sth}	4	4.6	5	V	A
1.6	V _S undervoltage threshold hysteresis		7	V _{Sth_hys}		0.2		V	A
2	RXD Output Pin (Open Drain)								
2.1	Low-level input current	Normal mode V _{LIN} = 0V, V _{RXD} = 0.4V	1	I _{R_{XD}L}	1.3	2.5	8	mA	A
2.2	RXD saturation voltage	5-kΩ pull-up resistor to 5V	1	V _{sat_{RXD}}			0.4	V	A
2.3	High-level leakage current	Normal mode V _{LIN} = V _{BAT} , V _{RXD} = 5V	1	I _{R_{XD}H}	-3		+3	μA	A
2.4	ESD zener diode	I _{RXD} = 100 μA	1	V _{Z_{RXD}}	5.8		8.6	V	A
3	TXD Input Pin								
3.1	Low-level voltage input		4	V _{TXDL}	-0.3		+0.8	V	A
3.2	High-level voltage input		4	V _{TXDH}	2		7	V	A
3.3	Pull-down resistor	V _{TXD} = 5V	4	R _{TXD}	125	250	600	kΩ	A
3.4	Low-level leakage current	V _{TXD} = 0V	4	I _{TXD}	-3		+3	μA	A
3.5	Low-level input current at local wake-up request	Pre-normal mode V _{LIN} = V _{BAT} , V _{WAKE} = 0V	4	I _{TXDwake}	1.3	2.5	8	mA	A
4	EN Input Pin								
4.1	Low-level voltage input		2	V _{ENL}	-0.3		+0.8	V	A
4.2	High-level voltage input		2	V _{ENH}	2		7	V	A
4.3	Pull-down resistor	V _{EN} = 5V	2	R _{EN}	125	250	600	kΩ	A
4.4	Low-level input current	V _{EN} = 0V	2	I _{EN}	-3		+3	μA	A
5	INH Output Pin								
5.1	High-level voltage	Normal mode I _{INH} = -200 μA	8	V _{INHH}	V _S - 0.8		V _S	V	A
5.2	High-level leakage current	Sleep mode V _{INH} = 27V, V _{Batt} = 27V	8	I _{INHL}	-3		+3	μA	A
6	WAKE Pin								
6.1	High-level input voltage		3	V _{WAKEH}	V _S - 1V		V _S + 0.3V	V	A
6.2	Low-level input voltage	I _{WAKE} = Typically -3 μA	3	V _{WAKEL}	-1V		V _S - 3V	V	A
6.3	Wake pull-up current	V _S < 27V	3	I _{WAKE}	-30	-10		μA	A
6.4	High-level leakage current	V _S = 27V, V _{WAKE} = 27V	3	I _{WAKE}	-5		+5	μA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter



6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = -40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7	LIN Bus Driver								
7.1	Driver recessive output voltage	R _{LOAD} = 500Ω / 1 kΩ	6	V _{BUSrec}	0.9 × V _S		V _S	V	A
7.2	Driver dominant voltage V _{BUSdom_DRV_LoSUP}	V _{VS} = 7V, R _{load} = 500Ω	6	V _{LoSUP}			1.2	V	A
7.3	Driver dominant voltage V _{BUSdom_DRV_HISUP}	V _{VS} = 18V, R _{load} = 500Ω	6	V _{HiSUP}			2	V	A
7.4	Driver dominant voltage V _{BUSdom_DRV_LoSUP}	V _{VS} = 7V, R _{load} = 1000Ω	6	V _{LoSUP_1k}	0.6			V	A
7.5	Driver dominant voltage V _{BUSdom_DRV_HISUP}	V _{VS} = 18V, R _{load} = 1000Ω	6	V _{HiSUP_1k}	0.8			V	A
7.6	Pull-up resistor to V _S	The serial diode is mandatory	6	R _{LIN}	20	30	60	kΩ	A
7.7	LIN current limitation V _{BUS} = V _{BAT_max}		6	I _{BUS_LIM}	40	120	200	mA	A
7.8	Input leakage current at the receiver, including pull-up resistor as specified	Input leakage current Driver off V _{BUS} = 0V, V _{Batt} = 12V	6	I _{BUS_PAS_dom}	-1			mA	A
7.9	Leakage current LIN recessive	Driver off 8V < V _{BAT} < 18V 8V < V _{BUS} < 18V V _{BUS} ≥ V _{BAT}	6	I _{BUS_PAS_rec}		15	20	μA	A
7.10	Leakage current at ground loss; Control unit disconnected from ground; Loss of local ground must not affect communication in the residual network	GND _{Device} = V _S V _{BAT} = 12V 0V < V _{BUS} < 18V	6	I _{BUS_NO_gnd}	-10	+0.5	+10	μA	A
7.11	Node has to sustain the current that can flow under this condition; Bus must remain operational under this condition	V _{BAT} disconnected V _{SUP_Device} = GND 0V < V _{BUS} < 18V	6	I _{BUS}		5	15	μA	A
8	LIN Bus Receiver								
8.1	Center of receiver threshold	V _{BUS_CNT} = (V _{th_dom} + V _{th_rec}) / 2	6	V _{BUS_CNT}	0.475 × V _S	0.5 × V _S	0.525 × V _S	V	A
8.2	Receiver dominant state	V _{EN} = 5V	6	V _{BUSdom}	-27		0.4 × V _S	V	A
8.3	Receiver recessive state	V _{EN} = 5V	6	V _{BUSrec}	0.6 × V _S		40	V	A
8.4	Receiver input hysteresis	V _{HYS} = V _{th_rec} - V _{th_dom}	6	V _{BUSHYS}	0.028 × V _S	0.1 × V _S	0.175 × V _S	V	A
8.5	Pre-wake detection LIN High-level input voltage		6	V _{LINH}	V _S - 1V		V _S + 0.3V	V	A
8.6	Pre-wake detection LIN Low-level input voltage	Switches the LIN receiver on	6	V _{LINL}	-27V		V _S - 3.3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

6. Electrical Characteristics (Continued)

5V < V_S < 27V, T_j = -40°C to +150°C

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
9	Internal Timers								
9.1	Dominant time for wake-up via LIN bus	V _{LIN} = 0V	6	T _{BUS}	30	90	150	μs	A
9.2	Time of low pulse for wake-up via pin WAKE	V _{WAKE} = 0V	3	T _{WAKE}	7	35	50	μs	A
9.3	Time delay for mode change from pre-normal mode to normal mode via pin EN	V _{EN} = 5V	2	T _{norm}	2	7	15	μs	A
9.4	Time delay for mode change from normal mode into sleep mode via pin EN	V _{EN} = 0V	2	T _{sleep}	2	7	12	μs	A
9.5	TXD dominant time out timer	V _{TXD} = 0V	4	T _{dom}	6	9	20	ms	A
9.6	Power-up delay between V _S = 5V until INH switches to high	V _{VS} = 5V		T _{VS}			200	μs	A
10	LIN Bus Driver (see Figure 6-1 on page 12) Bus load conditions: Load1, small, 1 nF 1 kΩ; Load2, big, 10 nF 500Ω; R _{RXD} = 5 kΩ; C _{RXD} = 20 pF; The following two rows specify the timing parameters for proper operation at 20.0 kBits/s.								
10.1	Duty cycle 1	TH _{Rec(max)} = 0.744 × V _S TH _{Dom(max)} = 0.581 × V _S V _S = 7.0V to 18V t _{Bit} = 50 μs D1 = t _{bus_rec(min)} / (2 × t _{Bit})		D1	0.396				A
10.2	Duty cycle 2	TH _{Rec(min)} = 0.422 × V _S TH _{Dom(min)} = 0.284 × V _S V _S = 7.0V to 18V t _{Bit} = 50 μs D2 = t _{bus_rec(max)} / (2 × t _{Bit})		D2			0.581		A
10.3	Duty cycle 3	TH _{Rec(max)} = 0.778 × V _S TH _{Dom(max)} = 0.616 × V _S V _S = 7.0V to 18V t _{Bit} = 96 μs D3 = t _{bus_rec(min)} / (2 × t _{Bit})	LIN	D3	0.417				A
10.4	Duty cycle 4	TH _{Rec(max)} = 0.389 × V _S TH _{Dom(max)} = 0.251 × V _S V _S = 7.0V to 18V t _{Bit} = 96 μs D4 = t _{bus_rec(min)} / (2 × t _{Bit})	LIN	D4			0.590		A
11	Receiver Electrical AC Parameters of the LIN Physical Layer LIN receiver, RXD load conditions (C _{RXD}): 20 pF, R _{pull-up} = 5 kΩ								
11.1	Propagation delay of receiver (see Figure 6-1 on page 12)	t _{rec_pd} = max(t _{rx_pdr} , t _{rx_pdf}) V _S = 7.0V to 18V		t _{rx_pd}			6	μs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	t _{rx_sym} = t _{rx_pdr} - t _{rx_pdf} V _S = 7.0V to 18V		t _{rx_sym}	-2		+2	μs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 6-1. Definition of Bus Timing Parameter

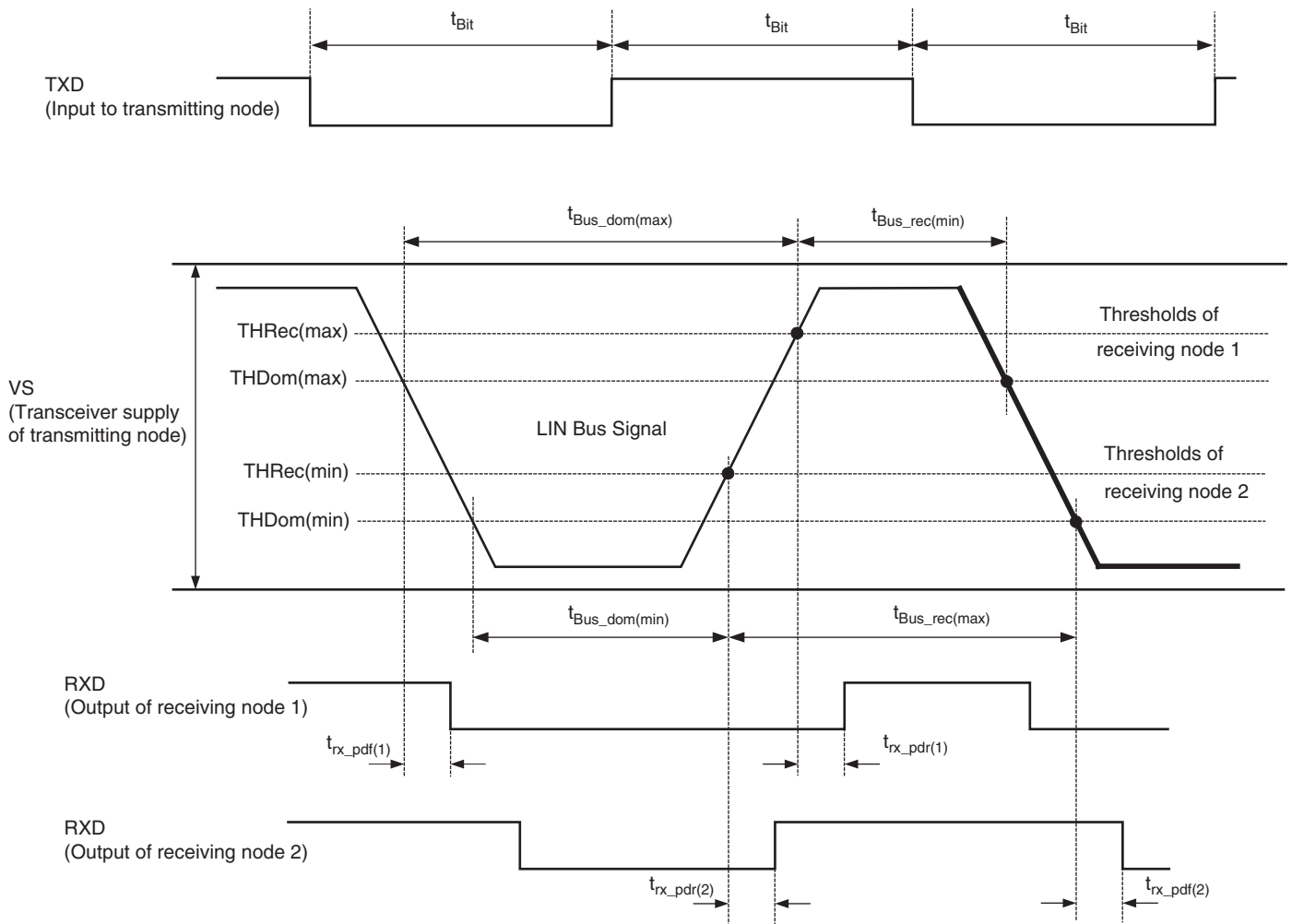
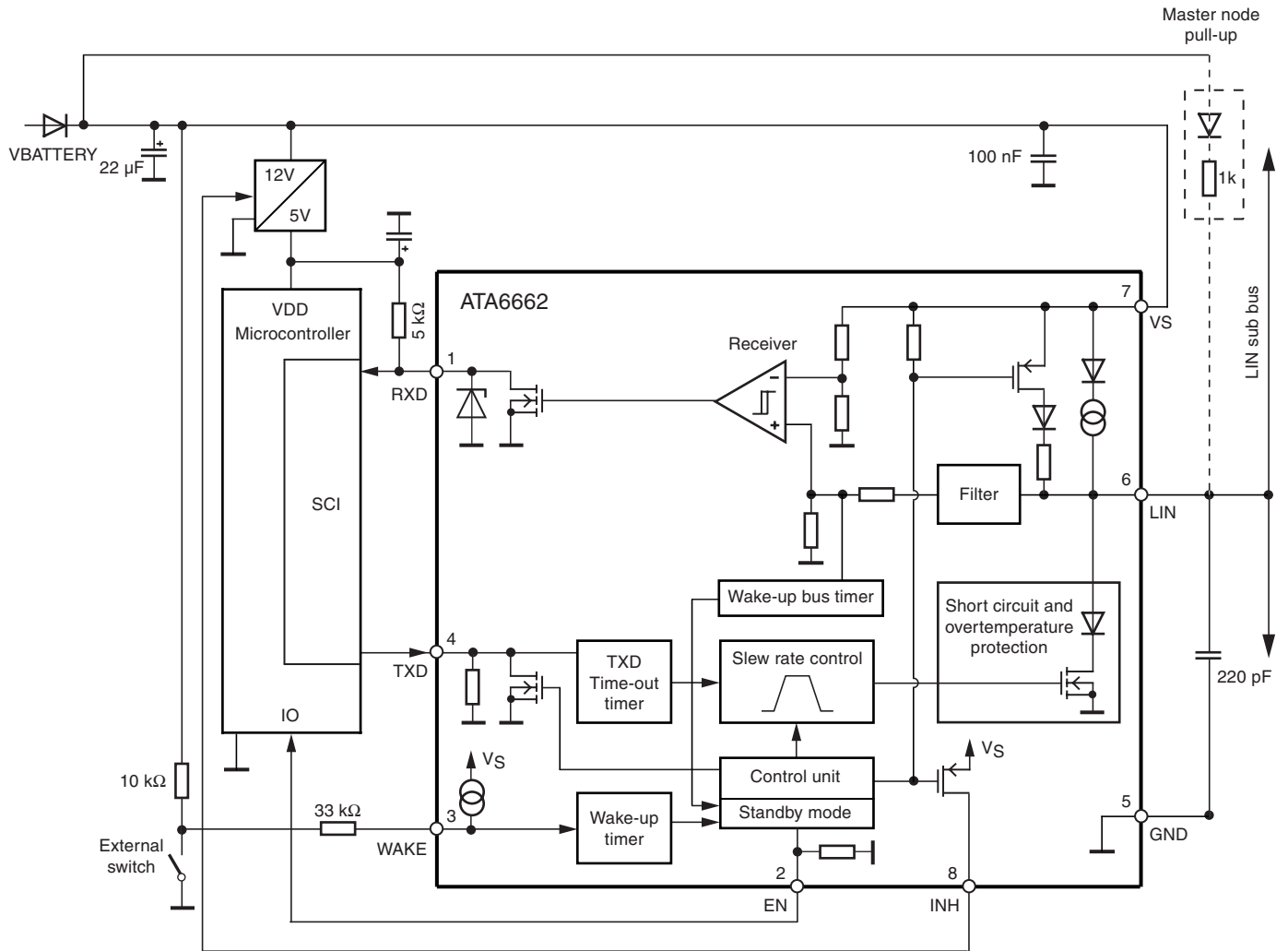


Figure 6-2. Application Circuit



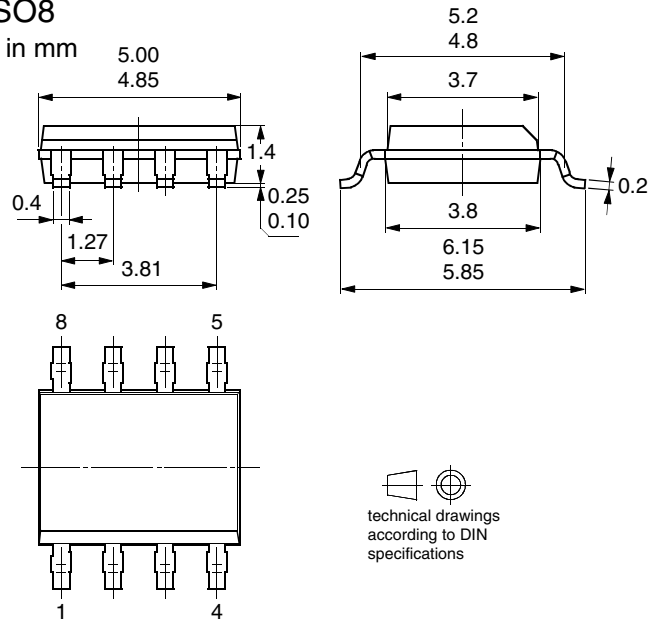
7. Ordering Information

Extended Type Number	Package	Remarks
ATA6662-TAQY	SO8	LIN transceiver, Pb-free

8. Package Information

Package SO8

Dimensions in mm



9. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4916E-AUTO-02/07	<ul style="list-style-type: none"> • Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 2 “Electrical Characteristics” on pages 9 to 11 changed
4916D-AUTO-02/07	<ul style="list-style-type: none"> • Features on page 1 changed • Section 1 “Description” on page 1 changed • Table 2-1 “Pin Description” on page 2 changed • Section 3.2 “Ground Pin (GND)” on page 3 changed • Section 3.7 “Enable Input Pin (EN)” on page 4 changed • Section 3.11 “Remote Wake-up via Dominant Bus State” on page 5 changed • Figure 3-1 “Mode of Operation” on page 6 changed • Section 3-14 “Fail-safe Features” on page 6 changed • Section 4 “Absolute Maximum Ratings” on page 8 changed • Section 6 “Electrical Characteristics” on pages 9 to 11 changed



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Atmel Operations

Memory

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Literature Requests

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