International
IOR Rectifier

Data Sheet No. PD-6.032C

IR2131

3 HIGH SIDE AND 3 LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 high side & 3 low side drivers
- Matched propagation delay for all channels
- Outputs out of phase with inputs

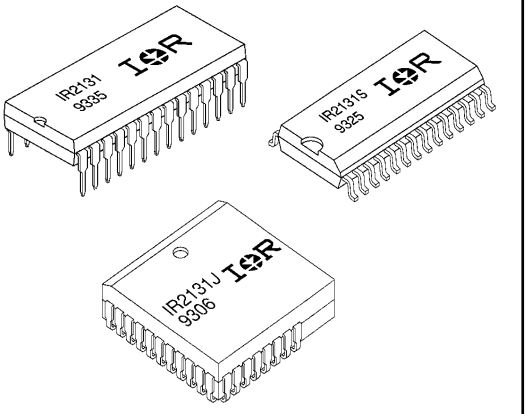
Product Summary

V_{OFFSET}	600V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	1.3 & 0.6 µs
Deadtime (typ.)	700 ns

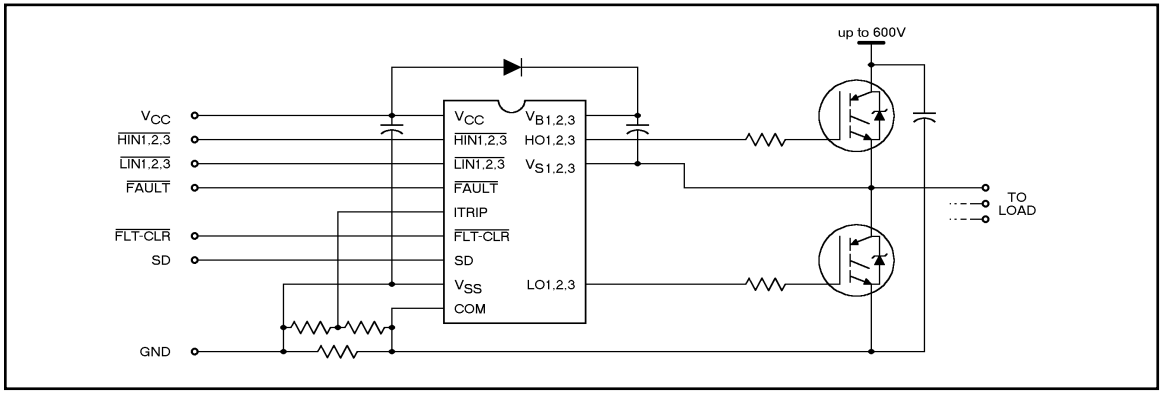
Description

The IR2131 is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A current trip function which terminates all six outputs can be derived from an external current sense resistor. A shutdown input is provided for a customized shutdown function. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that any of the shutdowns has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 600 volts.

Packages



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional Information is shown in Figures 7 through 10.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	-0.3	525	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Low Side and Logic Fixed Supply Voltage	-0.3	25	
V_{SS}	Logic Ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT\text{-}CLR}$, SD & ITRIP)	V_{SS} - 0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
P_D	Package Power Dissipation @ $T_A \leq +25°C$ (28 Lead DIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 Lead PLCC)	—	2.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (28 Lead DIP)	—	83	°C/W
	(28 Lead SOIC)	—	78	
	(44 Lead PLCC)	—	63	
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Offset Voltage	Note 1	600	
$V_{HO1,2,3}$	High Side Floating Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side and Logic Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage ($\overline{HIN1,2,3}$, $\overline{LIN1,2,3}$, $\overline{FLT\text{-}CLR}$, SD & ITRIP)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ Output Voltage	V_{SS}	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S of -5V to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 4 through 5.

Symbol	Parameter Definition	Value Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	0.6	1.3	2.0	µs	V_{IN} = 0 & 5V, $V_{S1,2,3}$ = 0 to 600V
t_{off}	Turn-Off Propagation Delay	0.2	0.6	1.0		
t_r	Turn-On Rise Time	—	80	150	ns	
t_f	Turn-Off Fall Time	—	40	100		
t_{itrip}	ITRIP to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	400	—		V_{ITRIP} = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ Indication Delay	400	700	1000		V_{IN}, V_{ITRIP} = 0 & 5V
$t_{flt,in}$	Input Filter Time (All Six Inputs)	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{FLT\text{-}CLR}$ to $\overline{FAULT}$ Clear Time	400	700	1000		V_{IN}, V_{IT}, V_{FC} = 0&5V
t_{sd}	SD to Output Shutdown Propagation Delay	400	700	1000		V_{IN}, V_{SD} = 0 & 5V
DT	Deadtime	400	700	1200		V_{IN} = 0 & 5V

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: $\overline{HIN1,2,3}$ & $\overline{LIN1,2,3}$. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

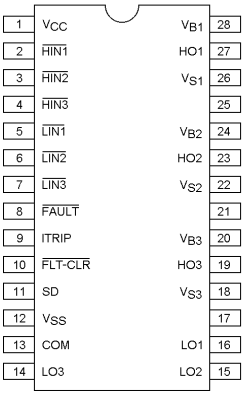
Symbol	Parameter Definition	Value Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	Shutdown Input Positive Going Threshold	1.2	1.8	2.1		
$V_{SD,TH-}$	Shutdown Input Negative Going Threshold	0.9	1.5	1.8		
$V_{IT,TH+}$	ITRIP Input Positive Going Threshold	250	485	600	mV	
$V_{IT,TH-}$	ITRIP Input Negative Going Threshold	200	400	550		
V_{OH}	High Level Output Voltage, V_{BIAS} - VO	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, VO	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} Supply Current	—	30	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	3.0	4.5	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	190	300	µA	V_{IN} = 0V
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	50	100		V_{IN} = 5V
I_{ITRIP+}	"High" ITRIP Bias Current	—	75	150		ITRIP = 5V
I_{ITRIP-}	"Low" ITRIP Bias Current	—	—	100	nA	ITRIP = 0V
I_{FCLR+}	Logic "1" Fault Clear Bias Current	—	125	250	µA	$\overline{FLT\text{-}CLR}$ = 0V
I_{FCLR-}	Logic "0" Fault Clear Bias Current	—	75	150		$\overline{FLT\text{-}CLR}$ = 5V
I_{SD+}	Logic "1" Shutdown Bias Current	—	75	150		SD = 5V
I_{SD-}	Logic "0" Shutdown Bias Current	—	—	100	nA	SD = 0V

Static Electrical Characteristics -- Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1,2,3 & LIN1,2,3. The V_O and I_O parameters are referenced to COM and $V_{S1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.

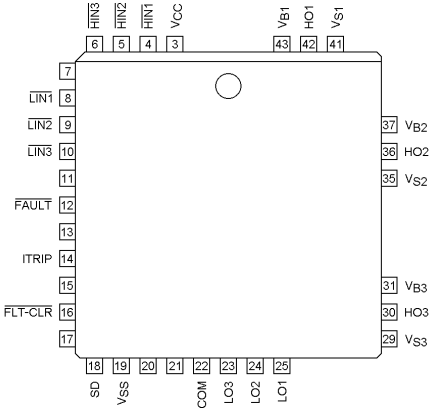
Parameter		Value				
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2	V	
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	8.2	8.7	9.2		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.8	8.3	8.8		
$R_{on,FLT}$	$\overline{FAULT}$ Low On-Resistance	—	55	75	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	200	250	—	mA	V_O = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	420	500	—		V_O = 15V, V_{IN} = 5V PW ≤ 10 µs

Lead Assignments



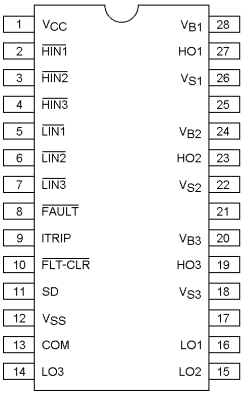
28 Lead DIP

IR2131



44 Lead PLCC w/o 12 Leads

IR2131J

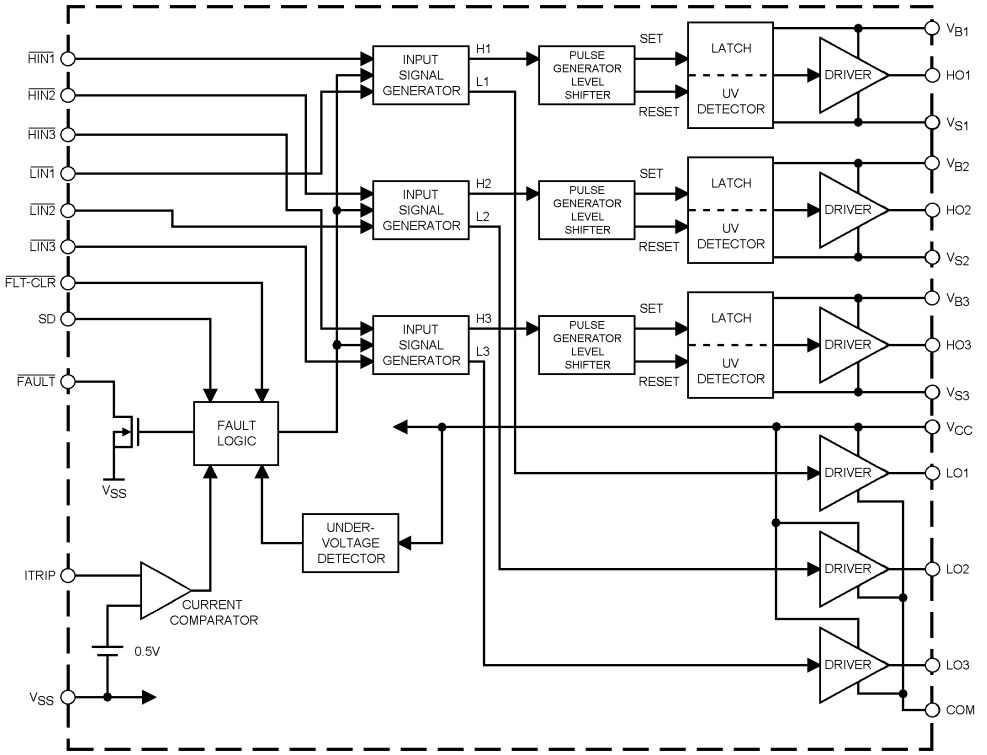


28 Lead SOIC (Wide Body)

IR2131S

Part Number

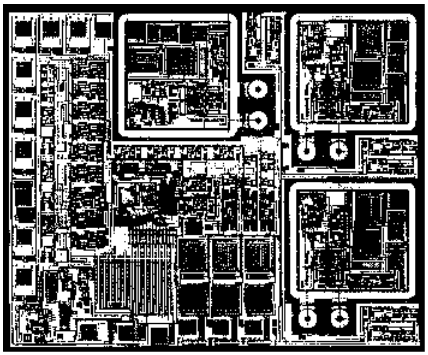
Functional Block Diagram



Lead Definitions

Lead Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FLT-CLR}$	Logic input for fault clear
SD	Logic input for shutdown
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
COM	Low side return

Device Information

Process & Design Rule			HVDCMOS 4.0 µm
Transistor Count			700
Die Size			167 X 141 X 26 (mil)
Die Outline			
Thickness of Gate Oxide			800Å
Connections		Material	Poly Silicon
	First Layer	Width	4 µm
		Spacing	6 µm
		Thickness	5000Å
		Material	Al - Si (Si: 1.0% ±0.1%)
	Second Layer	Width	6 µm
		Spacing	9 µm
		Thickness	20,000Å
Contact Hole Dimension			8 µm X 8 µm
Insulation Layer		Material	PSG (SiO_2)
		Thickness	1.5 µm
Passivation		Material	PSG (SiO_2)
		Thickness	1.5 µm
Method of Saw			Full Cut
Method of Die Bond			Ablebond 84 - 1
Wire Bond		Method	Thermo Sonic
		Material	Au (1.0 mil / 1.3 mil)
Leadframe		Material	Cu
		Die Area	Ag
		Lead Plating	Pb : Sn (37 : 63)
Package		Types	28 Lead PDIP & SOIC / 44 Lead PLCC
		Materials	EME6300 / MP150 / MP190
Remarks:			

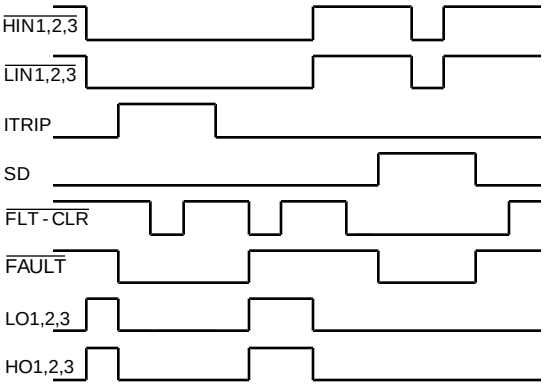


Figure 1. Input/Output Timing Diagram

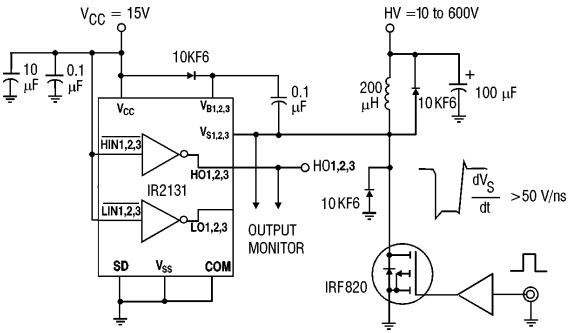


Figure 2. Floating Supply Voltage Transient Test Circuit

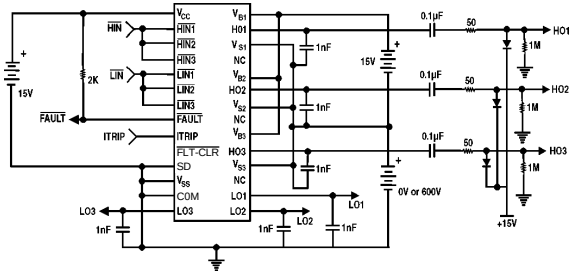


Figure 3. Switching Time Test Circuit

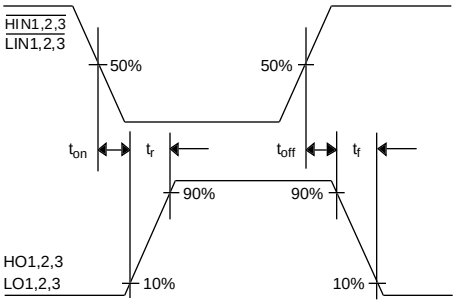


Figure 4. Switching Time Waveform Definitions

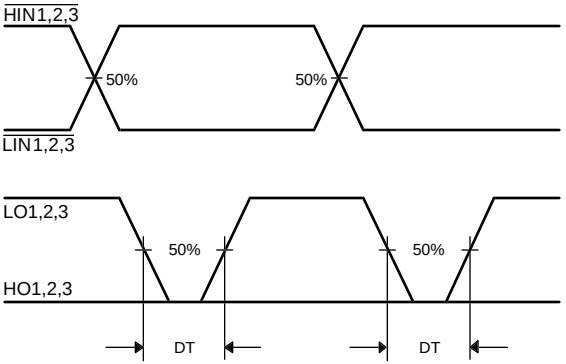


Figure 5. Deadtime Waveform Definitions

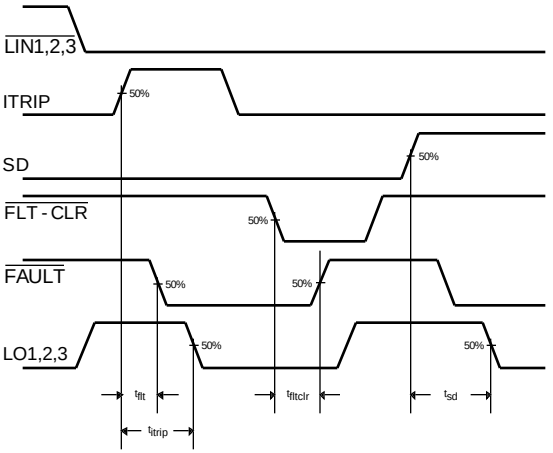


Figure 6. Shutdown Waveform Definitions

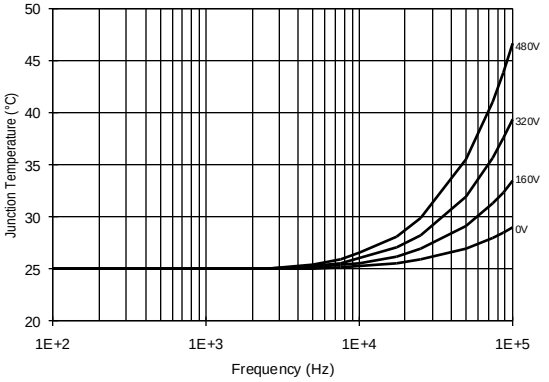


Figure 7. IR2131 T_J vs. Frequency (IRF820)
R_{GATE} = 33Ω, V_{CC} = 15V

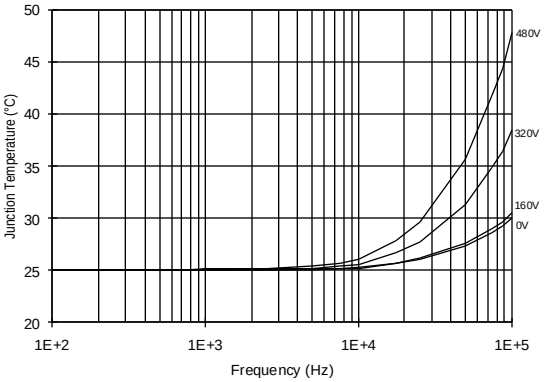


Figure 8. IR2131 T_J vs. Frequency (IRF830)
R_{GATE} = 20Ω, V_{CC} = 15V

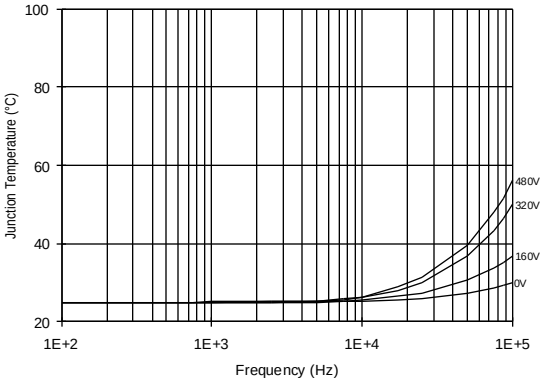


Figure 9. IR2131 T_J vs. Frequency (IRF840)
R_{GATE} = 15Ω, V_{CC} = 15V

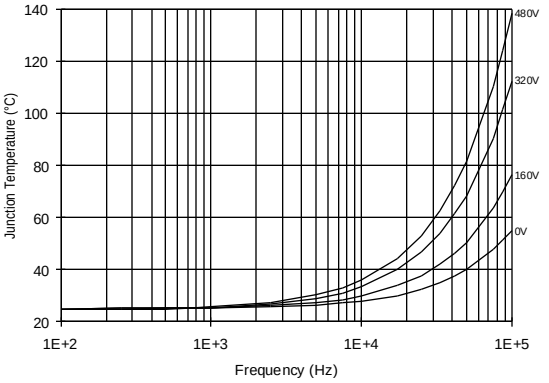


Figure 10. IR2131 T_J vs. Frequency (IRF450)
R_{GATE} = 10Ω, V_{CC} = 15V