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# KA3525A

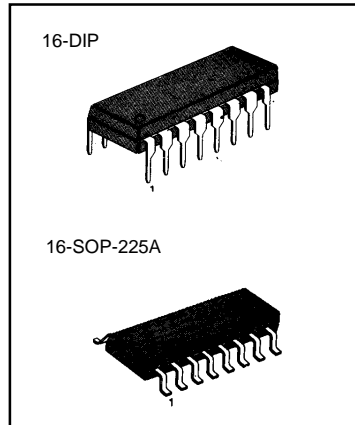
# SMPS CONTROLLER

## VOLTAGE-MODE PWM CONTROLLER

The KA3525A is a monolithic integrated circuit that included all of the control circuit necessary for a pulse width modulating regulator. There are a voltage reference, an error amplifier, a pulse width modulator, an oscillator, under-voltage lockout, soft start circuit, and output drivers in the chip.

### FEATURES

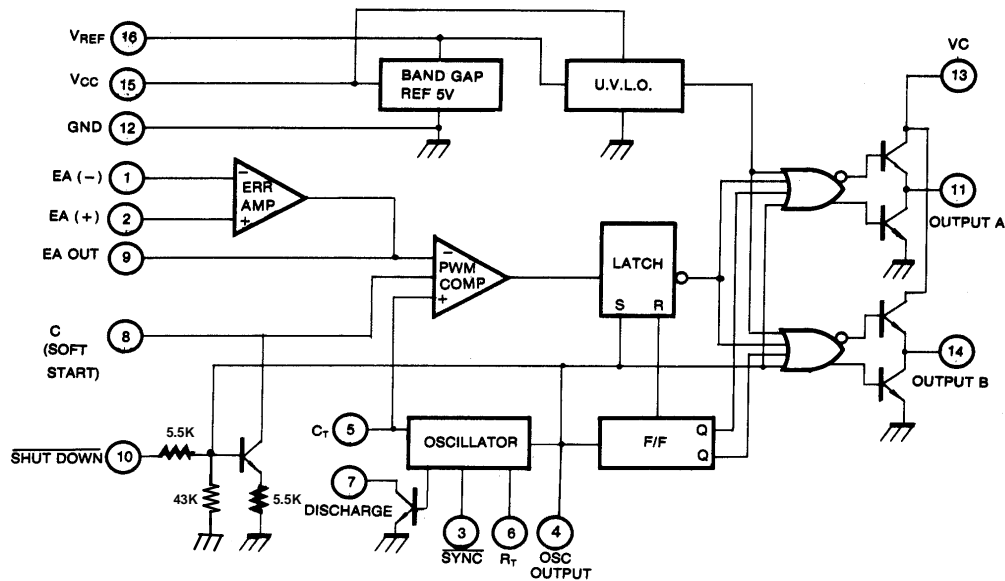
- $5V \pm 1\%$  Reference
- Oscillator Sync Terminal
- Internal Soft Start
- Deadtime Control
- Under-Voltage Lockout



### ORDERING INFORMATION

Device	Package	Operating Temperature
KA3525A	16 DIP	-30 ~ +85°C
KA3525AD	16-SOP-225A	-30 ~ +85°C

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	40	V
Collector Supply Voltage	$V_C$	40	V
Output Current, Sink or Source	$I_O$	500	mA
Reference Output Current	$I_{REF}$	50	mA
Oscillator Charging Current	$I_{CHG(OSC)}$	5	mA
Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_D$	1000	m/W
Operating Temperature	$T_{OPR}$	0 ~ +70	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65 ~ +150	$^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$T_{LEAD}$	+300	$^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = 20\text{V}$ ,  $T_A = -35^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>REFERENCE SECTION</b>						
Reference Output Voltage	$V_{REF}$	$T_J = 25^\circ\text{C}$	5.0	5.1	5.2	V
Line Regulation	$\Delta V_{REF}$	$V_{CC} = 8$ to $35\text{V}$		9	20	mV
Load Regulation	$\Delta V_{REF}$	$I_{REF} = 0$ to $20\text{mA}$		20	50	mV
Short Circuit Output Current	$I_{SC}$	$V_{REF} = 0$ , $T_J = 25^\circ\text{C}$		80	100	mA
Total Output Variation (Note 1)	$\Delta V_{REF}$	Line, Load and Temperature	4.95		5.25	V
Temperature Stability (Note 1)	$ST_T$			20	50	mV
Long Term Stability (Note 1)	$ST$	$T_J = 125^\circ\text{C}$ , 1 KH <sub>RS</sub>		20	50	mV
<b>OSCILLATOR SECTION</b>						
Initial Accuracy (Note 1, 2)	ACCUR	$T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 6$	%
Frequency Change With Voltage	$\Delta f/\Delta V_{CC}$	$V_{CC} = 8$ to $35\text{V}$ (Note 1, 2)		$\pm 0.8$	$\pm 2$	%
Maximum Frequency	$f_{(MAX)}$	$R_T = 2\text{K}\Omega$ , $C_T = 470\text{pF}$	400	430		KHz
Minimum Frequency	$f_{(MIN)}$	$R_T = 200\text{K}\Omega$ , $C_T = 0.1\mu\text{F}$		60	120	Hz
Clock Amplitude (Note 1, 2)	$V_{(CLK)}$		3	4		V
Clock Width (Note 1, 2)	$t_{W(CLK)}$	$T_J = 25^\circ\text{C}$	0.3	0.6	1	$\mu\text{s}$
Sync Threshold	$V_{TH(SYNC)}$		1.2	2	2.8	V
Sync Input Current	$I_{I(SYNC)}$	Sync = 3.5V		1.3	2.5	mA

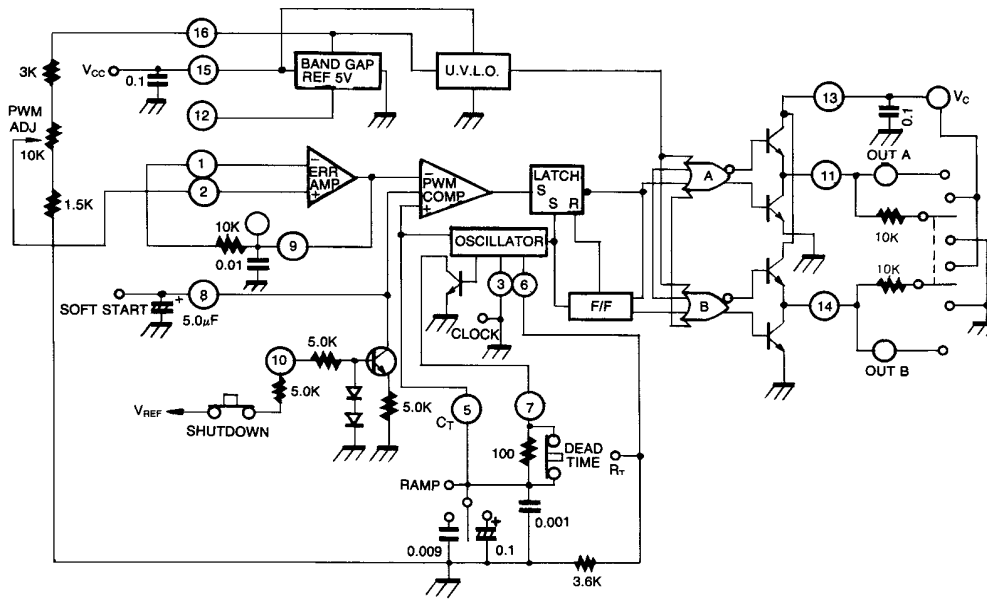
**ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub> = 20V, T<sub>A</sub> = -35°C to +85°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>ERROR AMPLIFIER SECTION (V<sub>CM</sub> = 5.1V)</b>						
Input Offset Voltage	V <sub>IO</sub>			1.5	10	mV
Input Bias Current	I <sub>BAIS</sub>			1	10	μA
Input Offset Current	I <sub>IO</sub>			0.1	1	μA
Open Loop Voltage Gain	G <sub>VO</sub>	R <sub>L</sub> ≥ 10MΩ	60	80		dB
Common Mode Rejection Ratio	CMRR	V <sub>CM</sub> = 1.5 to 5.2V	60	90		dB
Power Supply Rejection Ratio	PSRR	V <sub>CC</sub> = 8 to 3.5V	50	60		dB
<b>PWM COMPARATOR SECTION</b>						
Minimum Duty Cycle	D <sub>(MIN)</sub>				0	%
Maximum Duty Cycle	D <sub>(MAX)</sub>		45	49		%
Input Threshold Voltage (Note 2)	V <sub>TH1</sub>	Zero Duty Cycle	0.7	0.9		V
Input Threshold Voltage (Note 2)	V <sub>TH2</sub>	Max Duty Cycle		3.2	3.6	V
<b>SOFT-START SECTION</b>						
Soft Start Current	I <sub>SOFT</sub>	V <sub>SD</sub> = 0V, V <sub>SS</sub> = 0V	25	51	80	μA
Soft Start Low Level Voltage	V <sub>SL</sub>	V <sub>SD</sub> = 25V		0.3	0.7	V
Shutdown Threshold Voltage	V <sub>TH(SD)</sub>		0.7	1.3	1.7	V
Shutdown Input Current	I <sub>N(SD)</sub>	V <sub>SD</sub> = 2.5V		0.3	1	mA
<b>OUTPUT SECTION</b>						
Low Output Voltage I	V <sub>OL I</sub>	I <sub>SINK</sub> = 20mA		0.1	0.4	V
Low Output Voltage II	V <sub>OL II</sub>	I <sub>SINK</sub> = 100mA		0.05	2	V
High Output Voltage I	V <sub>CH I</sub>	I <sub>SOURCE</sub> = 20mA	18	19		V
High Output Voltage II	V <sub>CH II</sub>	I <sub>SOURCE</sub> = 100mA	17	18		V
Under Voltage Lockout	V <sub>UV</sub>	V <sub>8</sub> and V <sub>9</sub> = High	6	7	8	V
Collector Leakage Current	I <sub>LKG</sub>	V <sub>CC</sub> = 35V		80	200	μA
Rise Time (Note 1)	t <sub>R</sub>	C <sub>L</sub> = 1μF, T <sub>J</sub> = 26°C		80	600	nS
Fall Time (Note 1)	t <sub>F</sub>	C <sub>L</sub> = 1μF, T <sub>J</sub> = 25°C		70	300	nS
<b>STANDBY CURRENT</b>						
Supply Current	I <sub>CC</sub>	V <sub>CC</sub> = 35V		12	20	mA

(Note)

- These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production
- Tested at f<sub>OSC</sub> = 40 KHz (R<sub>T</sub> = 3.6K, C<sub>T</sub> = 0.01μF, R<sub>I</sub> = 0Ω)

TEST CIRCUIT



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