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تهران پاســاژ امجد طبقه1 واحد 16

02166766957 -02166766927

info@atrinelec.com

@atrinelec

Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N–Channel Enhancement–Mode Silicon Gate

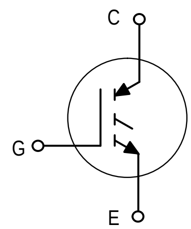
MGY40N60

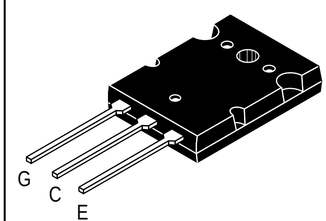
Motorola Preferred Device

IGBT IN TO–264
40 A @ 90°C
66 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operations at high frequencies.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	66 40 132	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	260 2.08	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.48 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc) Temperature Coefficient (Positive)		BV_{CES}	 600 —	 — 870	 — —	Vdc mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc) (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		I_{CES}	 — —	 — —	 100 2500	μAdc
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 20 Adc) (V_{GE} = 15 Vdc, I_C = 20 Adc, T_J = 125°C) (V_{GE} = 15 Vdc, I_C = 40 Adc)		$V_{CE(on)}$	 — — —	 2.20 2.10 2.60	 2.80 — 3.25	Vdc
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GE(th)}$	 4.0 —	 6.0 10	 8.0 —	Vdc mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 40 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	6810	—	pF
Output Capacitance		C_{oes}	—	464	—	
Transfer Capacitance		C_{res}	—	15	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	126	—	ns
Rise Time		t_r	—	95	—	
Turn–Off Delay Time		$t_{d(off)}$	—	530	—	
Fall Time		t_f	—	180	—	
Turn–Off Switching Loss		E_{off}	—	1.50	2.10	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	113	—	ns
Rise Time		t_r	—	104	—	
Turn–Off Delay Time		$t_{d(off)}$	—	588	—	
Fall Time		t_f	—	346	—	
Turn–Off Switching Loss		E_{off}	—	2.70	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc)	Q_T	—	248	—	nC
		Q_1	—	49	—	
		Q_2	—	81	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	 —	 13	 —	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

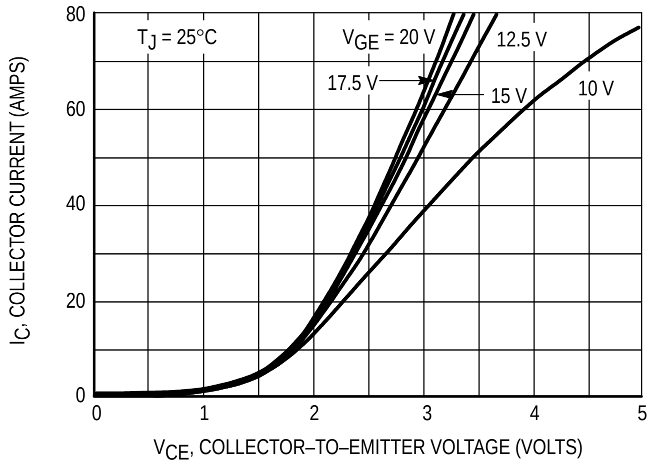


Figure 1. Output Characteristics, T_J = 25°C

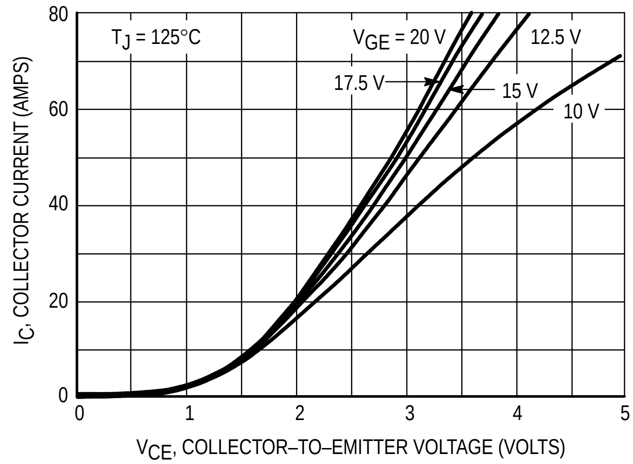


Figure 2. Output Characteristics, T_J = 125°C

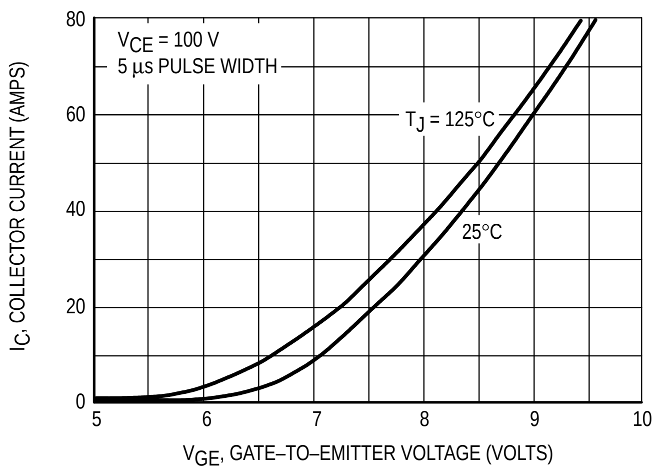


Figure 3. Transfer Characteristics

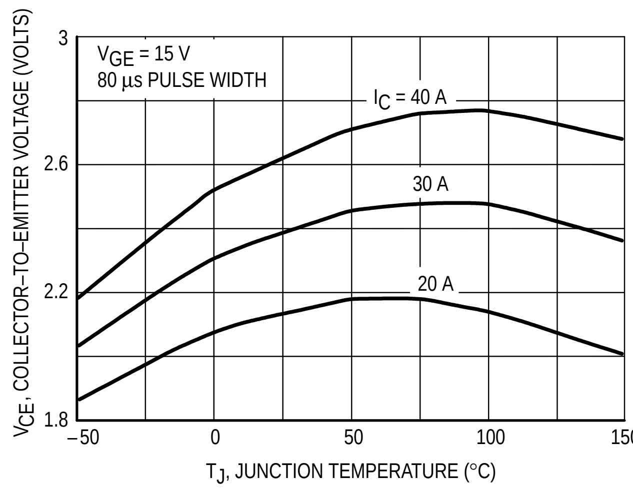


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

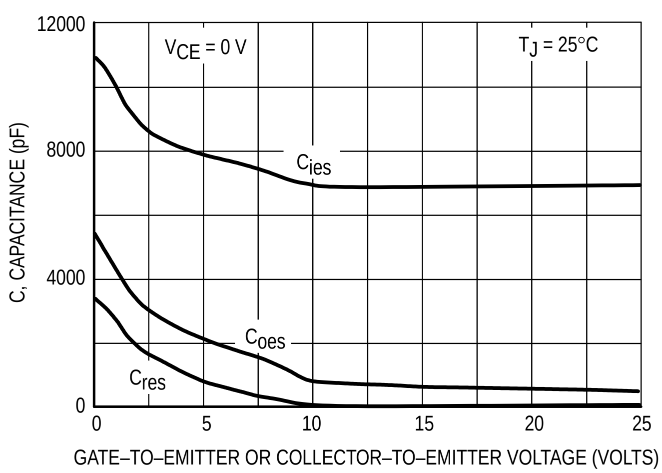


Figure 5. Capacitance Variation

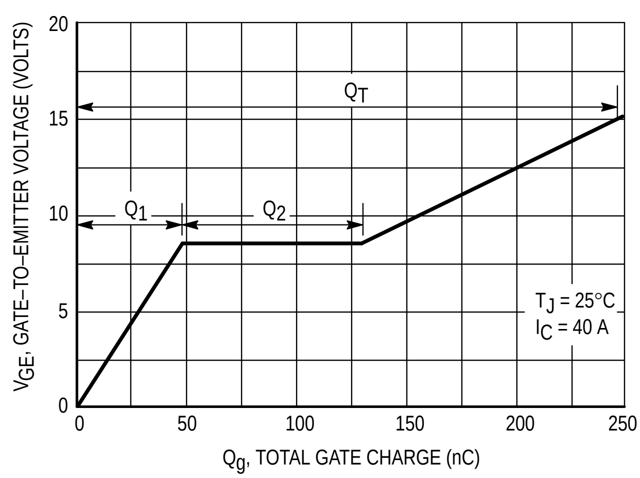


Figure 6. Gate–to–Emitter Voltage versus Total Charge

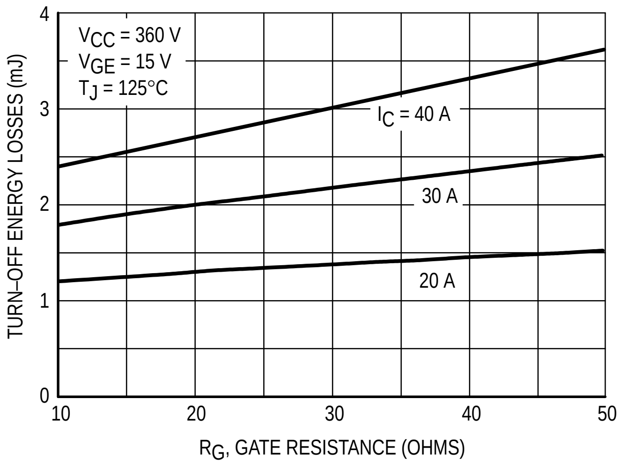


Figure 7. Turn–Off Losses versus Gate Resistance

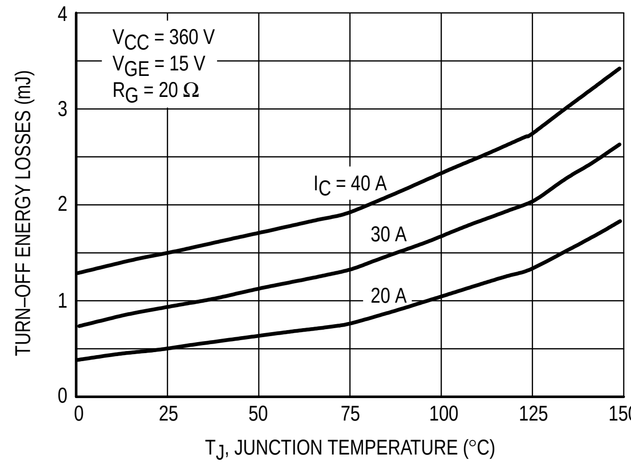


Figure 8. Turn–Off Losses versus Junction Temperature

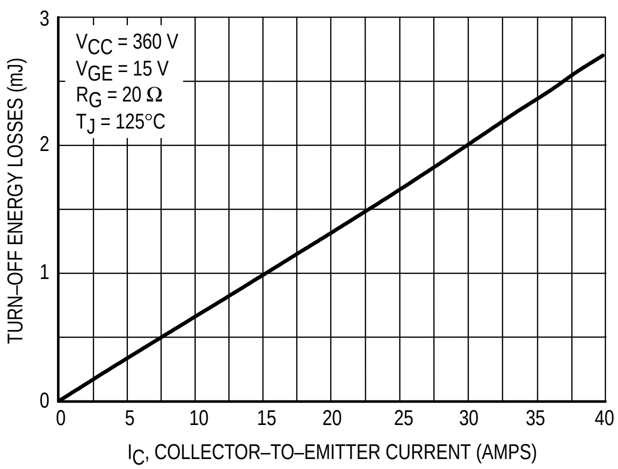


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

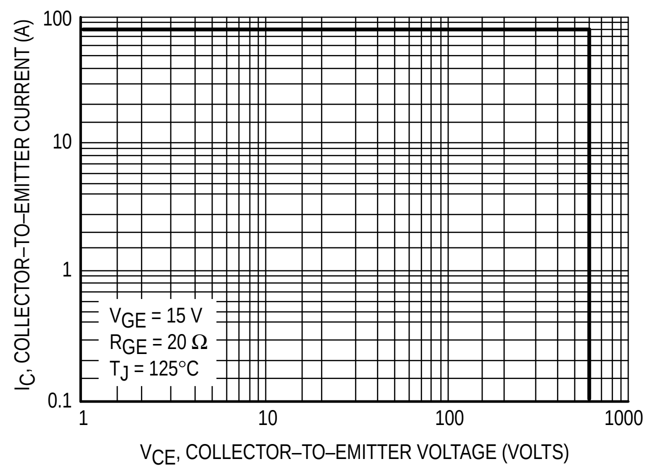
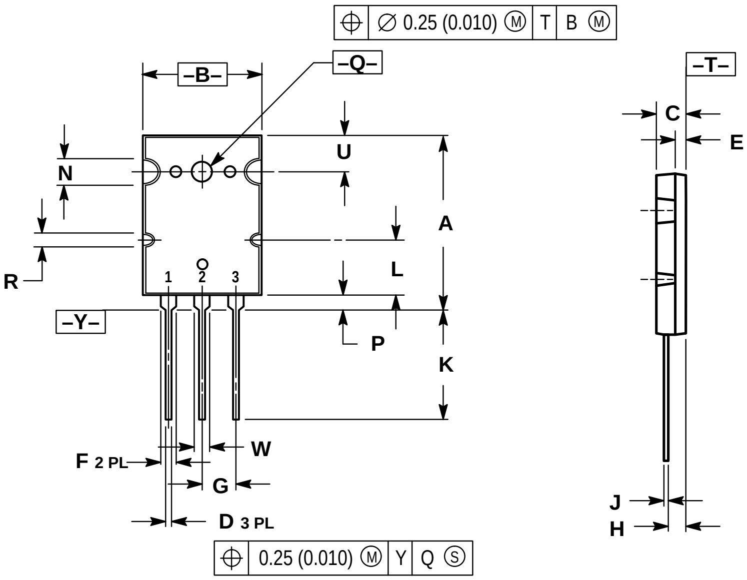


Figure 10. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

CASE 340G–02
TO–264
ISSUE E

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JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298