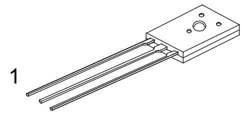
UTC MJE13002 NPN EPITAXIAL SILICON TRANSISTOR

NPN SILICON POWER TRANSISTOR

The UTC MJE13002 designed for use in high–volatge,high speed,power switching in inductive circuit, It is particularly suited for 115 and 220V switchmode applications such as switching regulator's,inverters,DC-DC converter,Motor control, Solenoid/Relay drivers and deflection circuits.



TO-126

1: BASE 2:COLLECTOR 3: EMITTER

FEATURES

*Collector-Emitter Sustaining Voltage:
V_{CEO} (sus)=300V.
*Collector-Emitter Saturation Voltage:
$V_{CE(sat)}$=1.0V(Max.) @Ic=1.0A, I_B =0.25A
*Switch Time- t_f =0.7 μs(Max.) @Ic=1.0A.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Collector-Emitter Voltage	V_{CEO} (sus)	300	V
Collector-Emitter Voltage	V_{CEV}	600	V
Emitter Base Voltage	V_{EBO}	9	V
Collector Current- Continuous - Peak (1)	I_C I_{CM}	1.5 3	A
Base Current – Continuous - Peak (1)	I_B I_{BM}	0.75 1.5	A
Emitter Current – Continuous - Peak (1)	I_E I_{EM}	2.25 4.5	A
Total Power Dissipation @ TA=25℃ Derate above 25℃	P_D	1.4 11.2	Watts MW/℃
Total Power Dissipation @ TC=25℃ Derate above 25℃	P_D	40 320	Watts MW/℃
Operating and Storage Junction Temperature Range	Tj , Tstg	-65 to +150	℃

THERMAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MAX	UNIT
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	℃/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	℃/W
Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	℃

(1) Pulse Test : Pulse Width=5ms,Duty Cycle≤10%

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Designer ' s Data for "Worst Case" Conditions – The Designer ' s Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves – representing boundaries on device characteristics – are given to facilitate "Worst case" design.

ELECTRICAL CHARACTERISTICS (Tc=25℃ unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (I_C=10 mA , I_B=0)	$V_{CEO(SUS)}$	300			V
Collector Cutoff Current (V_{CEV}=Rated Value, V_{BE} (off)=1.5 V) (V_{CEV}=Rated Value, VBE(off)=1.5V,Tc=100℃)	I_{CEV}			 1 5	mA
Emitter Cutoff Current (V_{EB}=9 V, Ic=0)	I_{EBO}			1	mA
SECOND BREAKDOWN					
Second Breakdown Collector Current with bass forward biased	Is/b	See Figure 10			
Clamped Inductive SOA with base reverse biased	RBSOA	See Figure 11			
ON CHARACTERISTICS (1)					
DC Current Gain (Ic=0.5 A, V_{CE}=2 V) (Ic=1 A, V_{CE}=2 V)	 h_{FE1} h_{FE2}	 8 5		 40 25	
Collector-Emitter Saturation Voltage (Ic=0.5A,I_B=0.1A) (Ic=1A,I_B=0.25A) (Ic=1.5A,I_B=0.5A) (Ic=1A,I_B=0.25A,Tc=100℃)	$V_{CE(sat)}$			 0.5 1 3 1	V
Base-Emitter Saturation Voltage (Ic=0.5A,I_B=0.1A) (Ic=1A,I_B=0.25 A) (Ic=1A,I_B=0.25A,Tc=100℃)	$V_{BE(sat)}$			 1 1.2 1.1	V
DYNAMIC CHARACTERISTICS					
Current-Gain-Bandwidth Product (Ic=100mA,V_{CE}=10 V, f=1MHz)	f_T	4	10		MHz
Output Capacitance (V_{CB}=10V,I_E=0,f=0.1MHz)	Cob		21		pF
SWITCHING CHARACTERISTICS(TABLE 1) (Vcc=125V,Ic=1A, IB1=IB2=0.2A,tp=25μs, Duty Cycle≤1%)					
Delay Time	t_d		0.05	0.1	μs
Rise Time	t_r		0.5	1	μs
Storage Time	t_s		2	4	μs
Fall Time	t_f		0.4	0.7	μs
INDUCTIVE LOAD, CLAMPED (TABLE 1,FIGURE 12) (Ic=1A,Vclamp=300V, I_{B1}=0.2A,V_{BE}(off)=5V,Tc=100℃)					
Storage Time	t_{sv}		1.7	4	μs
Crossover Time	t_c		0.29	0.75	μs
Fall Time	t_{fi}		0.15		μs

(1) Pulse Test : PW=300μs, Duty Cycle≤2%

CLASSIFICATION OF HFE1

RANK	A	B	C	D	E	F
RANGE	8 ~ 16	15 ~ 21	20 ~ 26	25 ~ 31	30 ~ 36	35 ~ 40

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 1. DC Current Gain

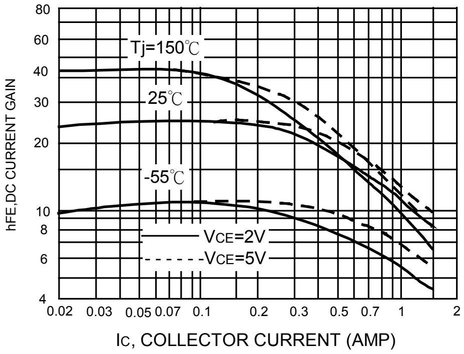


Figure 2. Collector Saturation Region

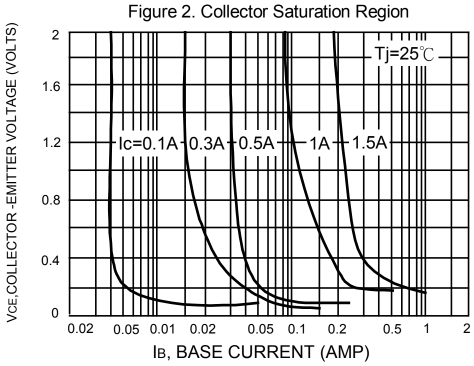


Figure 3. Base-Emitter Voltage

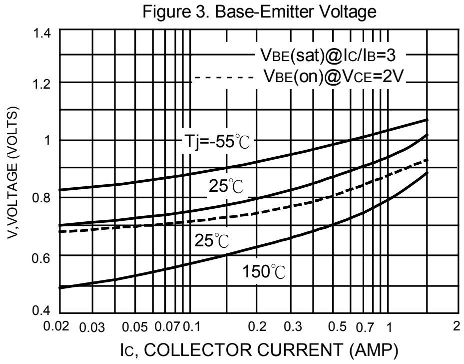


Figure 4. Collector-Emitter Saturation Region

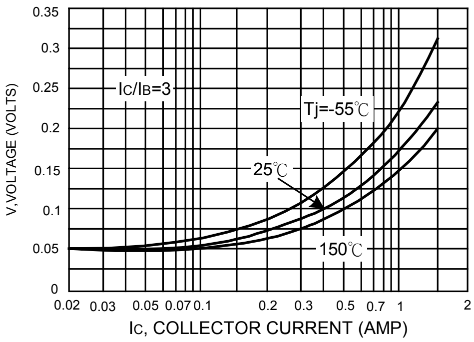


Figure 5. Collector Cutoff Region

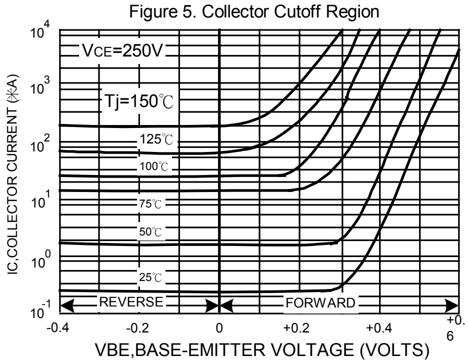


Figure 6. Capacitance

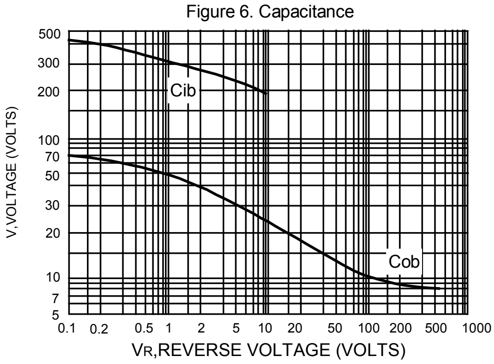


TABLE 1.TEST CONDITIONS FOR DYNAMIC PERFORMANCE

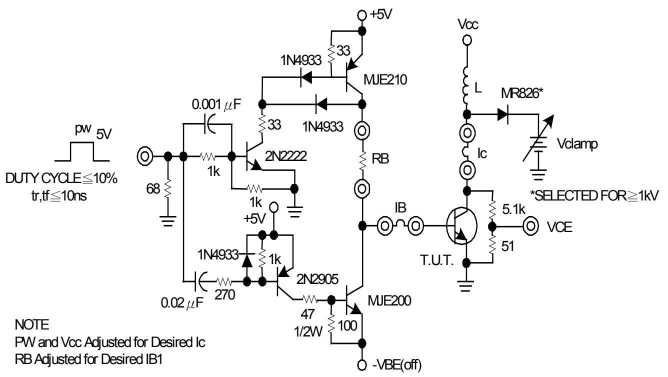
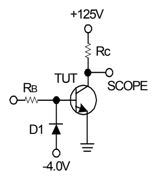
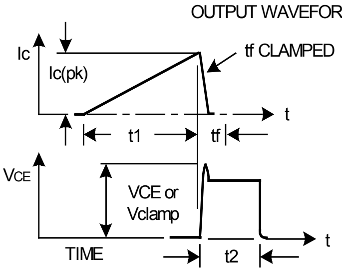
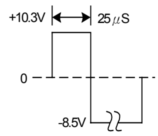
	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITHCING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data : FERROXCUBE core #6656 Full Bobbin (-200 Turns) #20 — GAP for 30 mH/2 A Lcoil=50mH — Vcc=20V Vclamp=300V	Vcc=125V Rc=125 Ω D1=1N5820 or Equiv. RB=47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t1 Adjusted to Obtain Ic $t1=\frac{Lcoil(Ic_{pk})}{Vcc}$ $t2=\frac{Lcoil(Ic_{pk})}{Vclamp}$ Test Equipment Scope-Tektronics 475 or Equivalent	 tr,tr<10ns Duty Cycly=1.0% RB and Rc adjusted for desired IB and Ic

TABLE 2.TYPICAL INDUCTIVE SWITCHING PERFORMANCE

Ic AMP	Tc ℃	Tsv μs	Trv μs	Tfi μs	Tti μs	Tc μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

Note: All Data Recorded in the inductive Switching Circuit Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase, However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each wave form to determine the total switching time, For this reason, the following new terms have been defined.

tsv=Voltage Storage Time, 90% I_{B1} to 10% Vclamp
trv=Voltage Rise Time, 10-90% Vclamp
tfi=Current Fall Time, 90-10% Ic
tti=Current Tail, 10-2% Ic
tc=Crossover Time, 10% Vclamp to 10% IC

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

PSWT=1/2 VccIc (tc)f

In general, trv + tfi≒tc. However, at lower test currents this relationship may not be valid.

As is common with most switching transistor, resistive switching is specified at 25℃ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (tc and tsv) which are guaranteed at 100 ℃

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second break-down. Safe operating area curves indicate Ic – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on Tc=25℃; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when Tc≧25℃. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case tem-perature by using the appropriate curve on Figure 12.

T_J(pk) may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during re-verse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an ava-lanche mode. Figure 11 gives RBSOA characteristics.

Figure 7. Inductive Switching Measurements

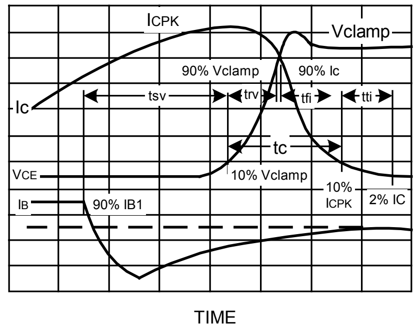


Figure 8. Turn-On Time

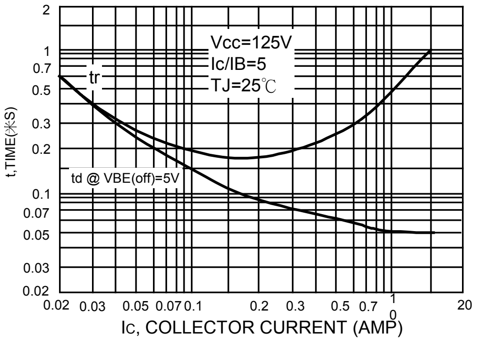


Figure 9. Turn-Off Time

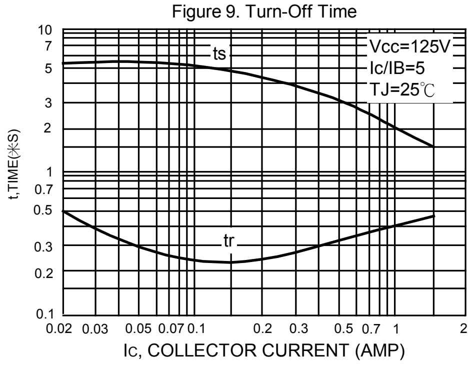


Figure 10. Active Region Safe Operating Area

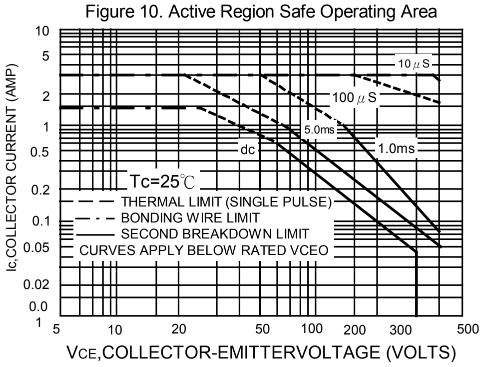


Figure 11. Reverse Bias Safe Operating Area

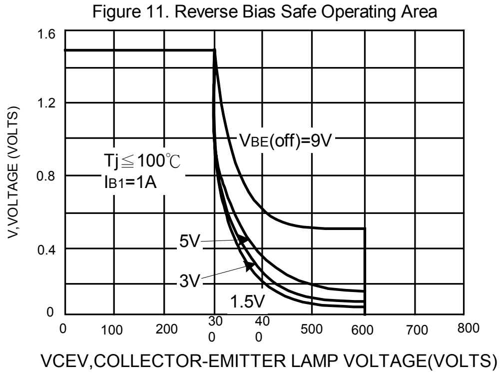


Figure 12. Forward Bias Power Derating

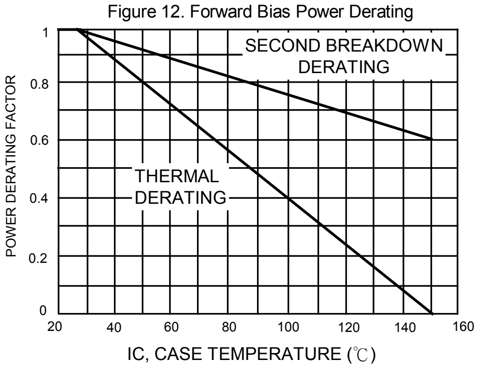


Figure 13. Thermal Response