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تهران، پاساژ امجد، طبقه اول، واحد ۱۶



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## 18A, 500V N-CHANNEL MOSFET

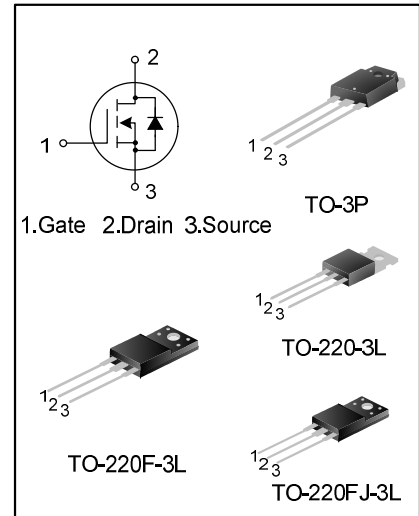
### GENERAL DESCRIPTION

SVF18N50F/T/PN/FJ is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ high-voltage planar VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

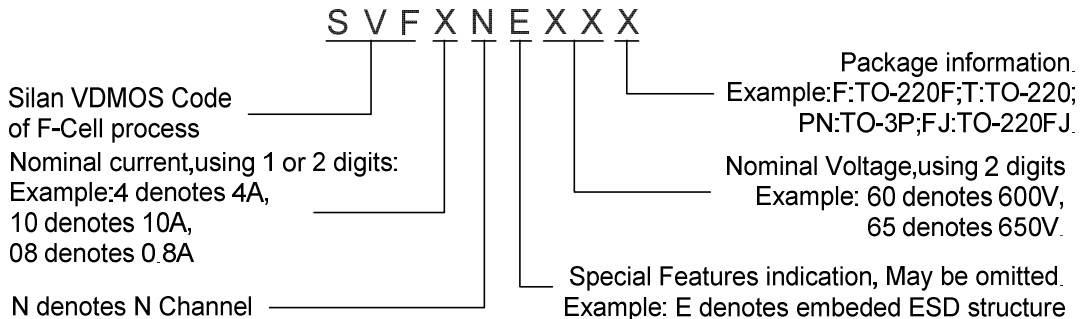
These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- 18A,500V, $R_{DS(on)(typ.)}=0.26\Omega@V_{GS}=10V$
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability



### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF18N50F	TO-220F-3L	SVF18N50F	Pb free	Tube
SVF18N50T	TO-220-3L	SVF18N50T	Pb free	Tube
SVF18N50PN	TO-3P	18N50	Pb free	Tube
SVF18N50FJ	TO-220FJ-3L	SVF18N50FJ	Halogen free	Tube

**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)**

Characteristics	Symbol	Ratings			Unit
		SVF18N50F/FJ	SVF18N50T	SVF18N50PN	
Drain-Source Voltage	V <sub>DS</sub>	500			V
Gate-Source Voltage	V <sub>GS</sub>	±30			V
Drain Current	I <sub>D</sub>	18			A
		11			
Drain Current Pulsed	I <sub>DM</sub>	72.0			A
Power Dissipation(T <sub>C</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	54	232	240	W
		0.43	1.86	1.92	W/°C
Single Pulsed Avalanche Energy (Note 1)	E <sub>AS</sub>	1502			mJ
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150			°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150			°C

**THERMAL CHARACTERISTICS**

Characteristics	Symbol	Ratings			Unit
		SVF18N50F/FJ	SVF18N50T	SVF18N50PN	
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	2.31	0.54	0.52	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	62.5	50	°C/W

**ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)**

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	500	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V	--	--	1.0	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A	--	0.26	0.31	Ω
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHZ	--	2320	--	pF
Output Capacitance	C <sub>OSS</sub>		--	282	--	
Reverse Transfer Capacitance	C <sub>RSS</sub>		--	7	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =250V, I <sub>D</sub> =18.0A, R <sub>G</sub> =25Ω  (Note 2,3)	--	60	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	131	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	115	--	
Turn-off Fall Time	t <sub>f</sub>		--	75	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =400V, I <sub>D</sub> =18.0A, V <sub>GS</sub> =10V  (Note 2,3)	--	38	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	12	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	12	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse p-n Junction Diode in the MOSFET	--	--	18.0	A
Pulsed Source Current	$I_{SM}$		--	--	72.0	
Diode Forward Voltage	$V_{SD}$	$I_S=18.0A, V_{GS}=0V$	--	--	1.3	V
Reverse Recovery Time	$T_{rr}$	$I_S=18.0A, V_{GS}=0V,$ $di_F/dt=100A/\mu s$ (Note 2)	--	583	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	7.1	--	$\mu C$

**Notes:**

1.  $L=30mH, I_{AS}=8.60A, V_{DD}=140V, R_G=25\Omega,$  starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

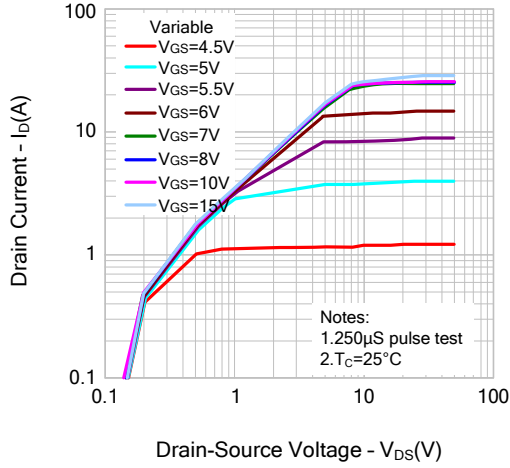


Figure 2. Transfer Characteristics

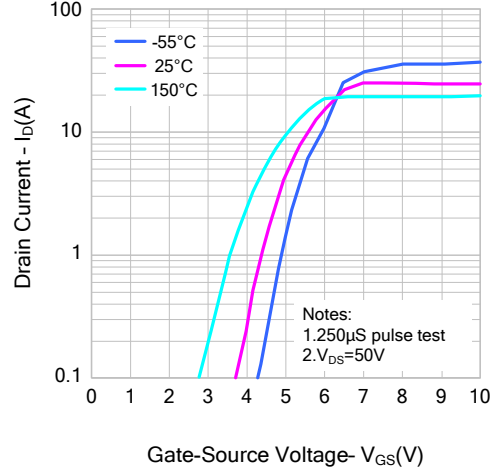


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

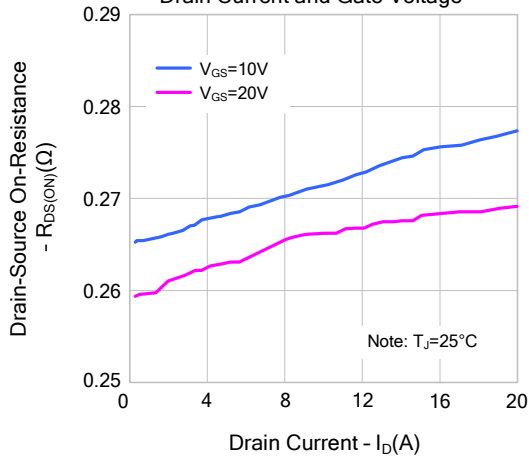


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

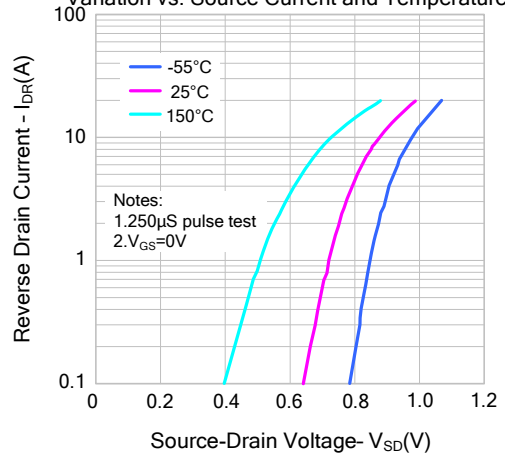


Figure 5. Capacitance Characteristics

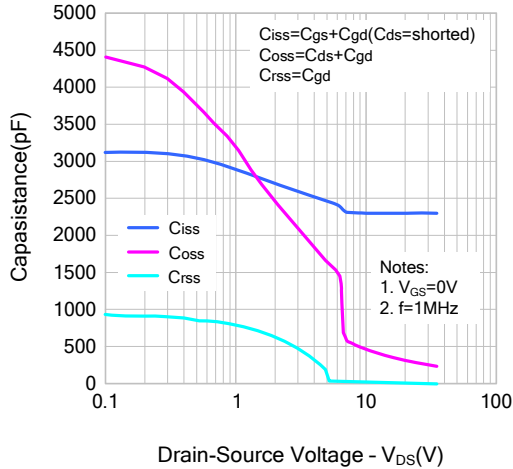
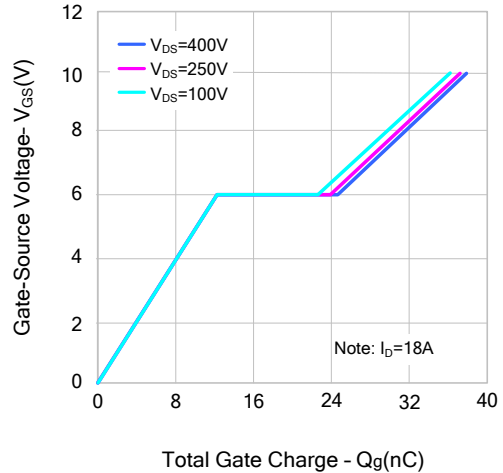


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS (continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

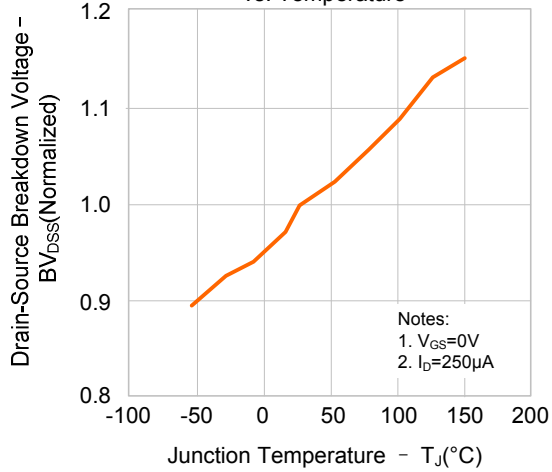


Figure 8. On-resistance Variation vs. Temperature

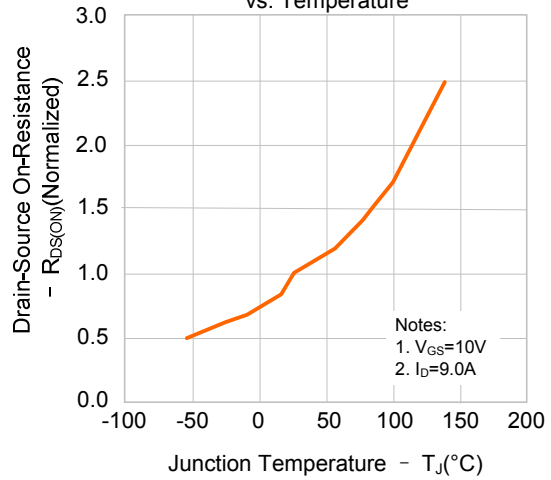


Figure 9-1. Max. Safe Operating Area(SVF18N50F/FJ)

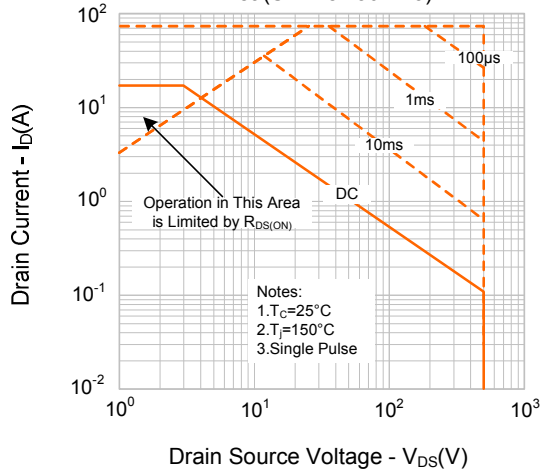


Figure 9-2. Max. Safe Operating Area(SVF18N50T)

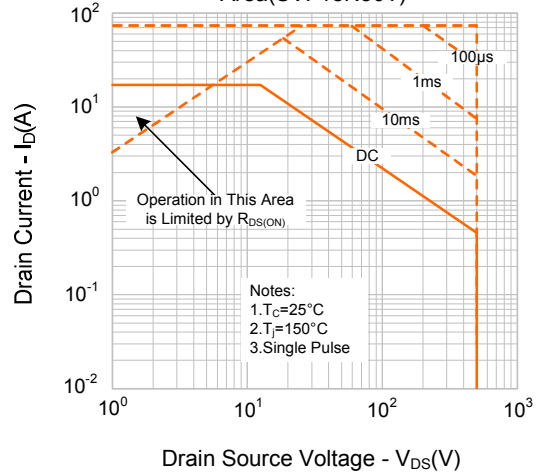


Figure 9-3. Max. Safe Operating Area(SVF18N50PN)

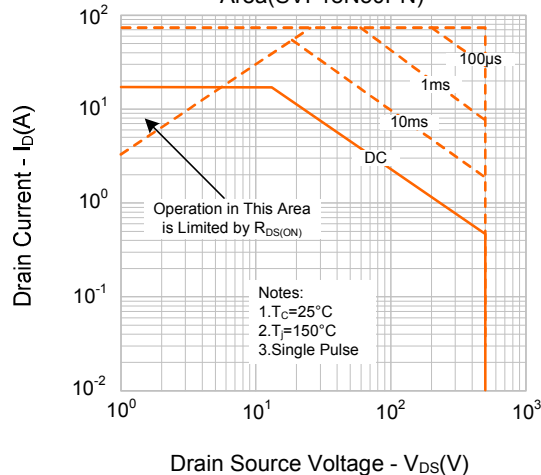
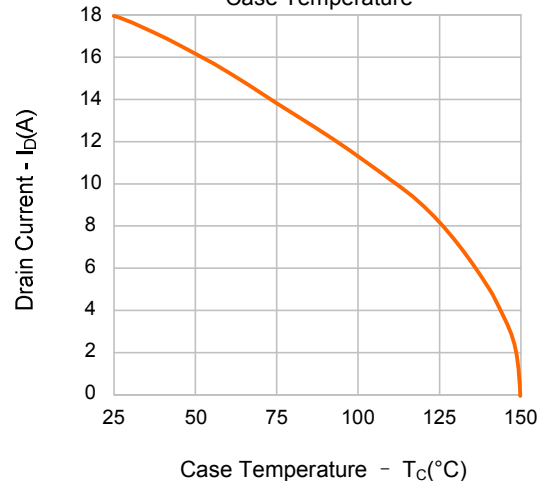
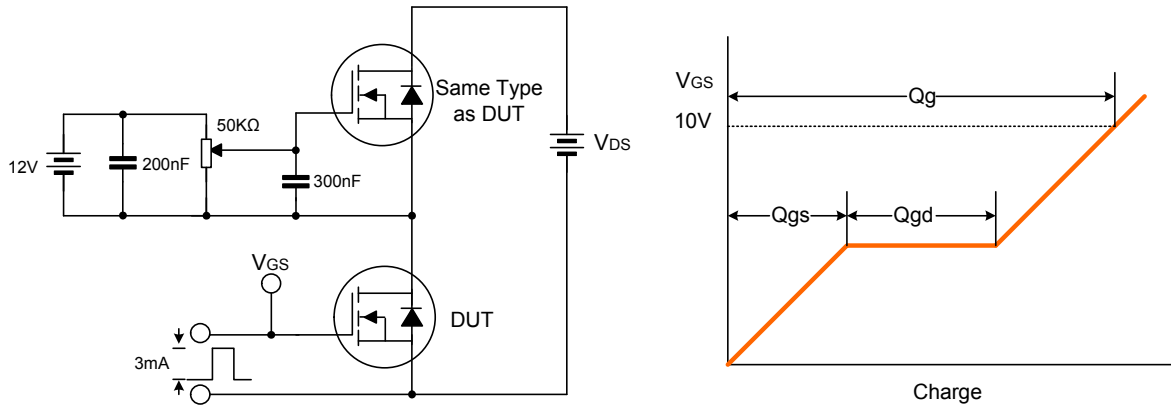


Figure 10. Maximum Drain Current vs. Case Temperature

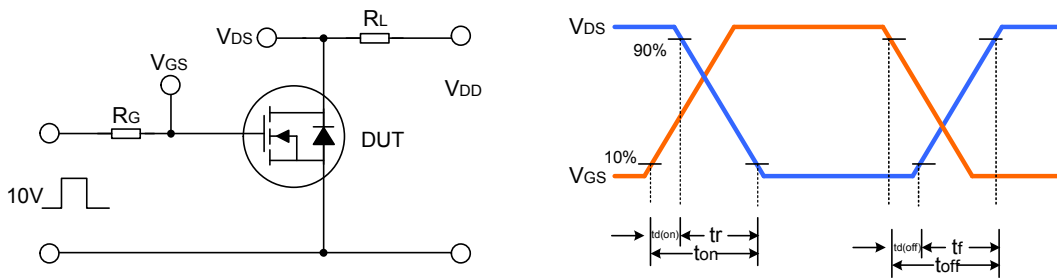


**TYPICAL TEST CIRCUIT**

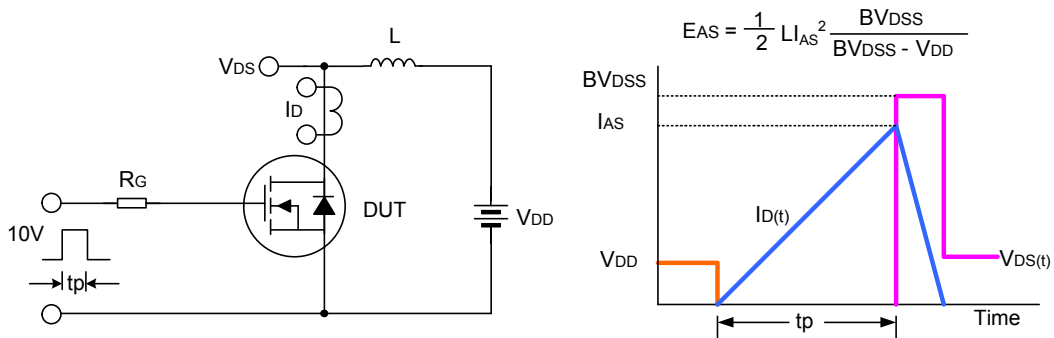
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



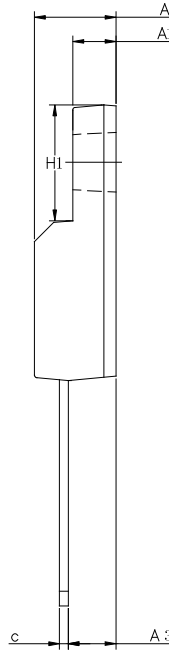
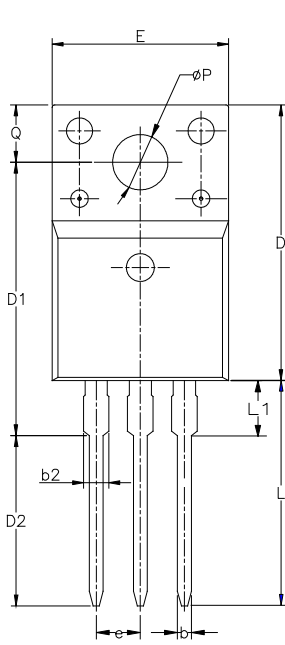
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

**TO-220F-3L**

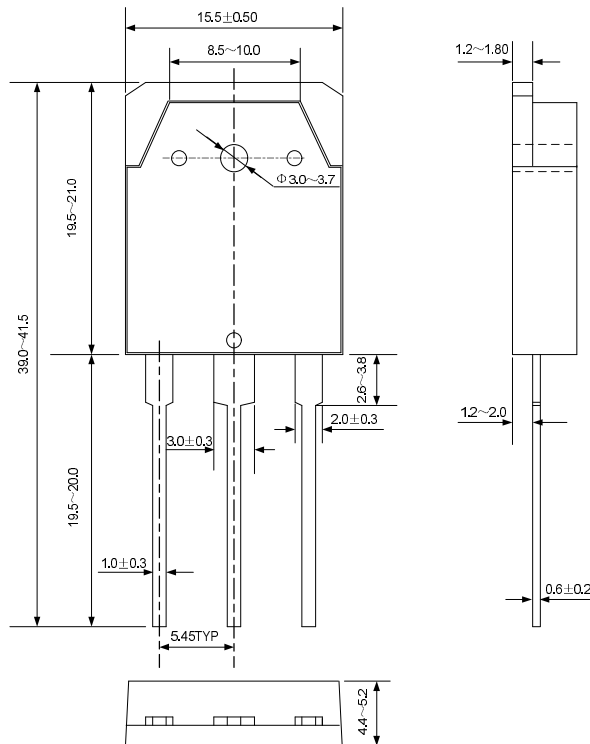
**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

**TO-3P**

**UNIT: mm**

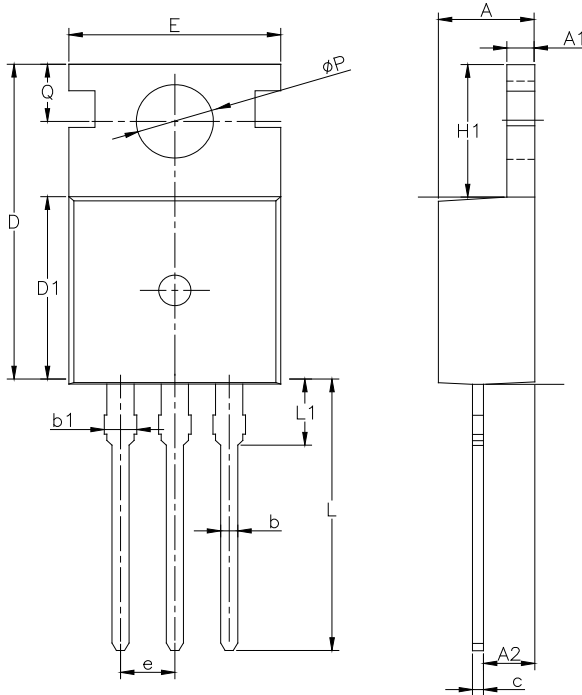




**PACKAGE OUTLINE(continued)**

**TO-220-3L**

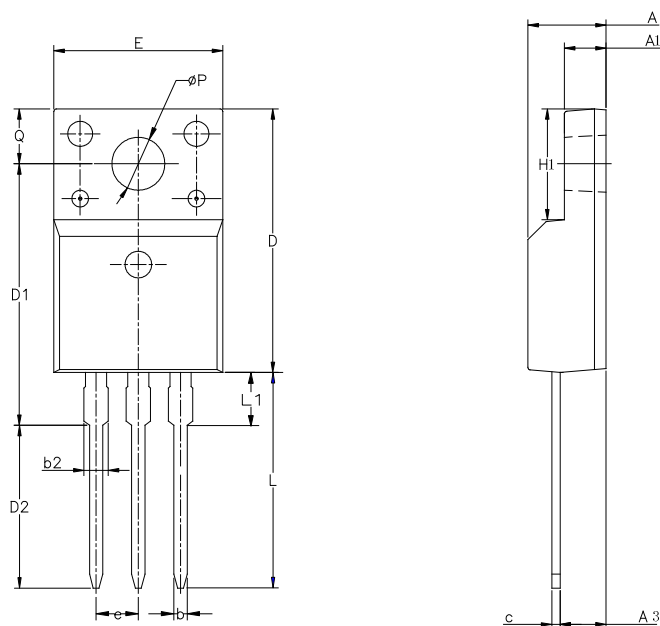
**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
$\phi P$	3.40	3.70	3.90
Q	2.60	—	3.20

**TO-220FJ-3L**

**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.55	0.70	0.85
b2	—	—	1.29
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	13.97	14.47	14.97
D2	10.58	11.08	11.58
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	—	—	2.00
$\phi P$	3.00	3.18	3.40
Q	3.05	3.30	3.55

**Disclaimer :**

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Rev.: 2.1

Revision History:

1. Add the package information of TO-220FJ-3L
  2. Update characteristics
- 

Rev.: 2.0

Revision History:

1. Modify the package information of TO-220-3L
- 

Rev.: 1.9

Revision History:

1. Modify the package information of TO-220F-3L
- 

Rev.: 1.8

Revision History:

1. Modify the thermal characteristics
- 

Rev.: 1.7

Revision History:

1. Modify the ordering information
- 

Rev.: 1.6

Revision History:

1. Change the schematic diagram of MOS
- 

Rev.: 1.5

Revision History:

1. Modify "TYPICAL CHARACTERISTICS"
- 

Rev.: 1.4

Revision History:

1. Modify the values of  $T_{rr}$  and  $Q_{rr}$
- 

Rev.: 1.3

Revision History:

1. Modify "TYPICAL CHARACTERISTICS"
- 

Rev.: 1.2

Revision History:

1. Add the package of TO-220-3L
-

Rev.: 1.1

Revision History:

1. Modify "PACKAGE OUTLINE"
- 

Rev.: 1.0

Revision History:

1. Original
- 
-