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تهران، پاساژ امجد، طبقه اول، واحد ۱۶



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## 7A, 650V N-CHANNEL MOSFET

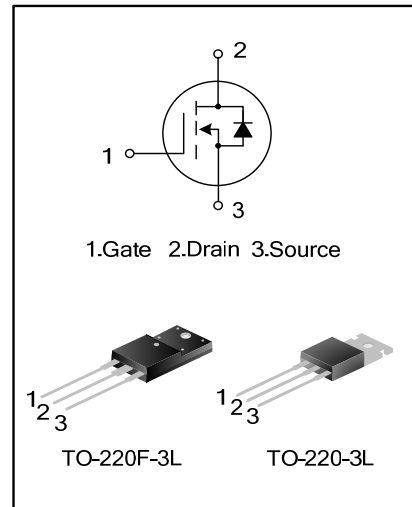
### GENERAL DESCRIPTION

SVF7N65T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

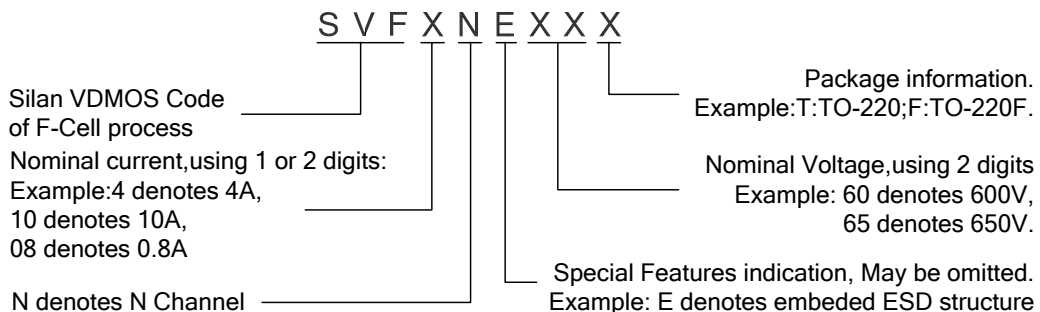
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

### FEATURES

- \* 7A,650V, $R_{DS(on)(typ)}=1.1\ \Omega@V_{GS}=10V$
- \* Low gate charge
- \* Low Crss
- \* Fast switching
- \* Improved dv/dt capability



### NOMENCLATURE



### ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF7N65T	TO-220-3L	SVF7N65T	Pb free	Tube
SVF7N65F	TO-220F-3L	SVF7N65F	Pb free	Tube

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Characteristics	Symbol	Ratings		Unit
		SVF7N65T	SVF7N65F	
Drain-Source Voltage	V <sub>DS</sub>	650		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current	I <sub>D</sub>	T <sub>C</sub> = 25°C		A
		T <sub>C</sub> = 100°C		
Drain Current Pulsed	I <sub>DM</sub>	28		A
Power Dissipation(T <sub>C</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	145	46	W
		1.16	0.37	
Single Pulsed Avalanche Energy (Note 1)	E <sub>AS</sub>	435		mJ
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150		°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150		°C

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF7N65T	SVF7N65F	
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.86	2.7	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	120	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B <sub>VDS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650	--	--	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V	--	--	10	μA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V	--	--	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A	--	1.1	1.4	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHZ	--	917.7	--	pF
Output Capacitance	C <sub>oss</sub>		--	98.6	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	1.90	--	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, R <sub>G</sub> =25Ω, I <sub>D</sub> =7.0A  (Note 2,3)	--	29.00	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	48.00	--	
Turn-off Delay Time	t <sub>d(off)</sub>		--	39.00	--	
Turn-off Fall Time	t <sub>f</sub>		--	33.00	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =520V, I <sub>D</sub> =7.0A, V <sub>GS</sub> =10V  (Note 2,3)	--	15.50	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	5.40	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	4.50	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	$I_{SM}$		--	--	28.0	
Diode Forward Voltage	$V_{SD}$	$I_S=7.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	$T_{rr}$	$I_S=7.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu S$ (Note 2)	--	365	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	3.4	--	$\mu C$

### Notes:

1.  $L=30mH, I_{AS}=5.0A, V_{DD}=100V, R_G=25\Omega,$  starting  $T_J=25^\circ C$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics

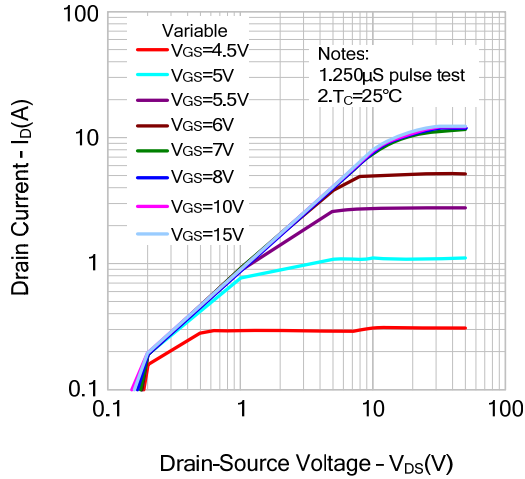


Figure 2. Transfer Characteristics

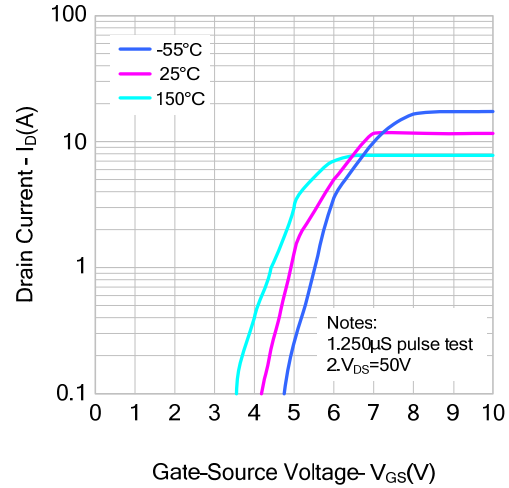


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

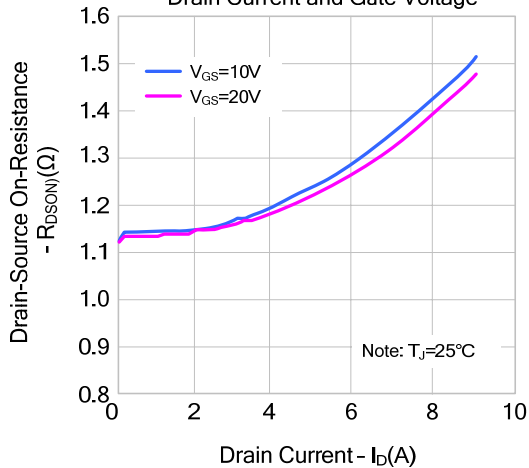


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

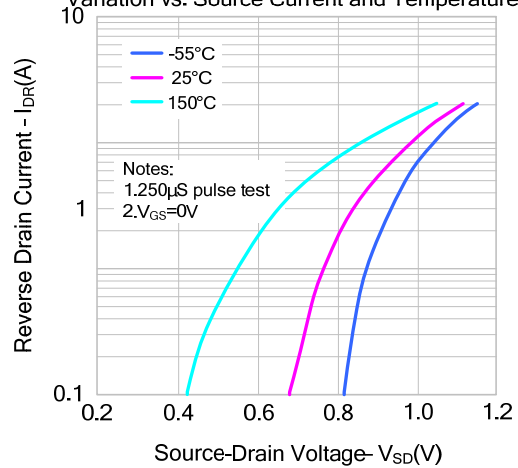


Figure 5. Capacitance Characteristics

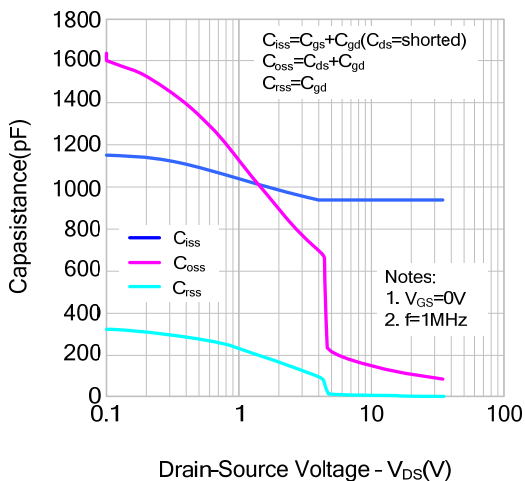
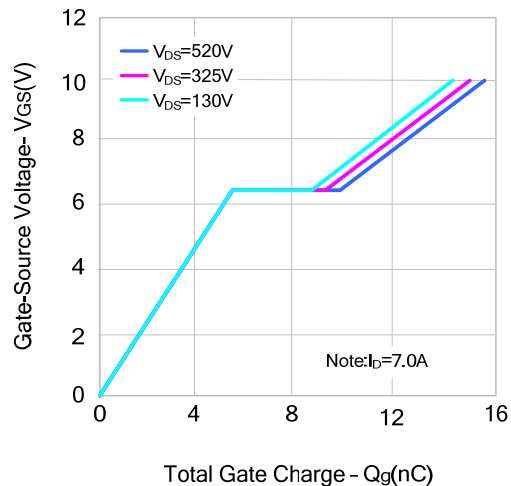


Figure 6. Gate Charge Characteristics



**TYPICAL CHARACTERISTICS(continued)**

Figure 7. Breakdown Voltage Variation vs. Temperature

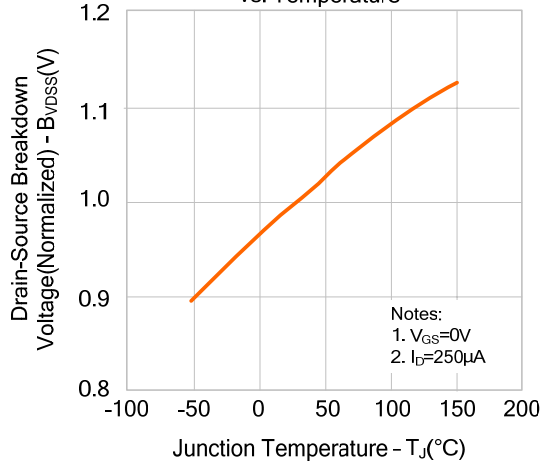


Figure 8. On-resistance Variation vs. Temperature

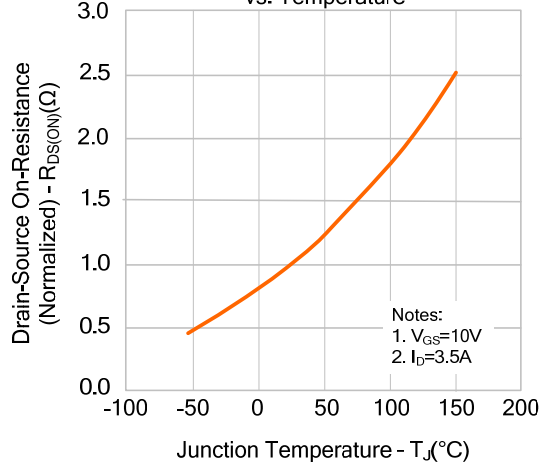


Figure 9-1. Max. Safe Operating Area(SVF7N65T)

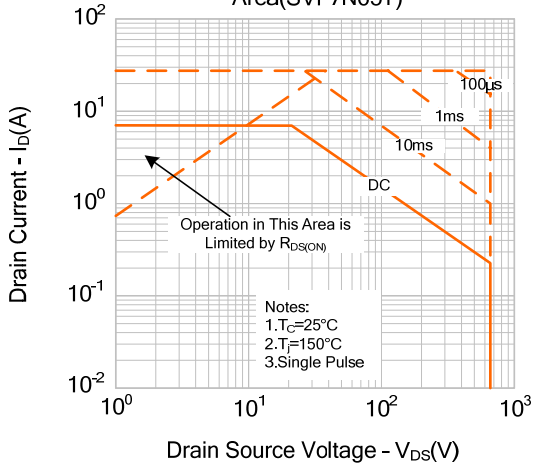


Figure 9-2. Max. Safe Operating Area(SVF7N65F)

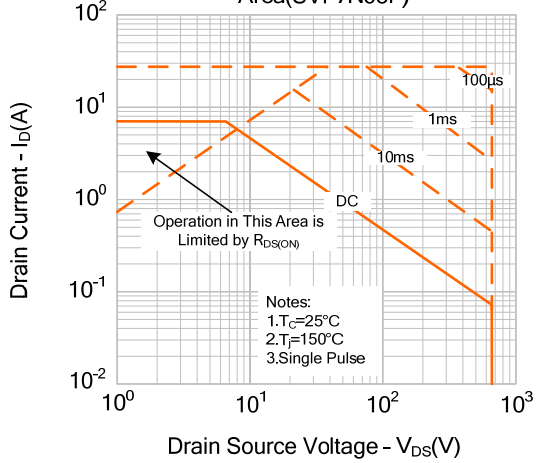
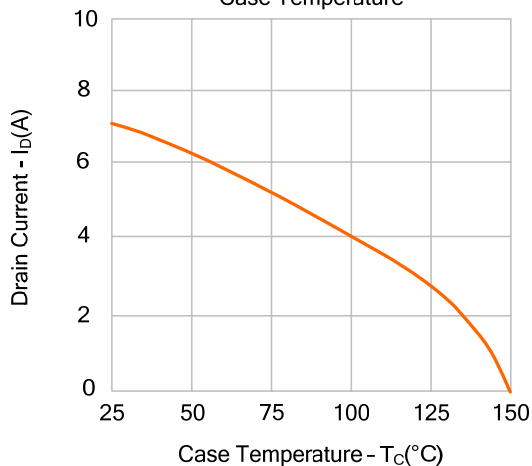
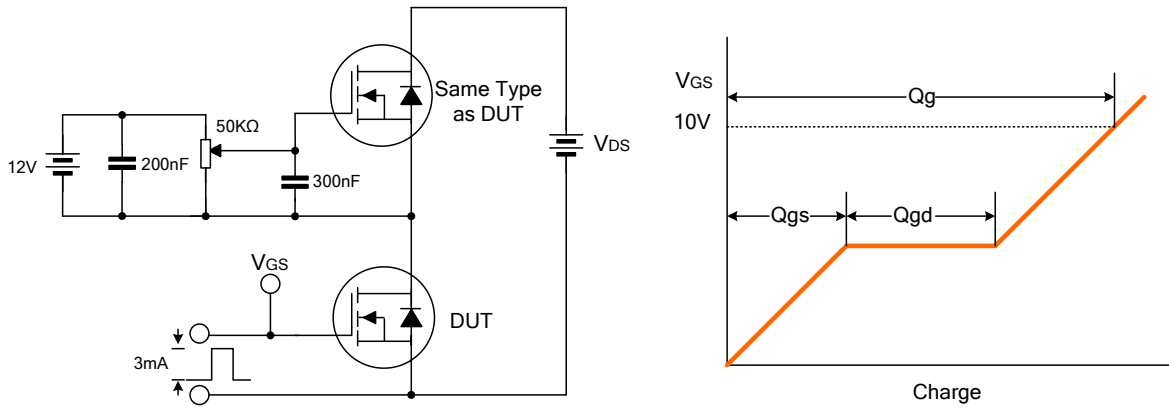


Figure 10. Maximum Drain Current vs. Case Temperature

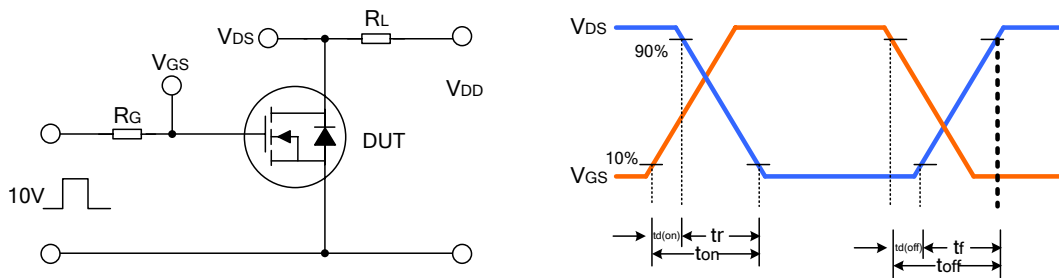


**TYPICAL TEST CIRCUIT**

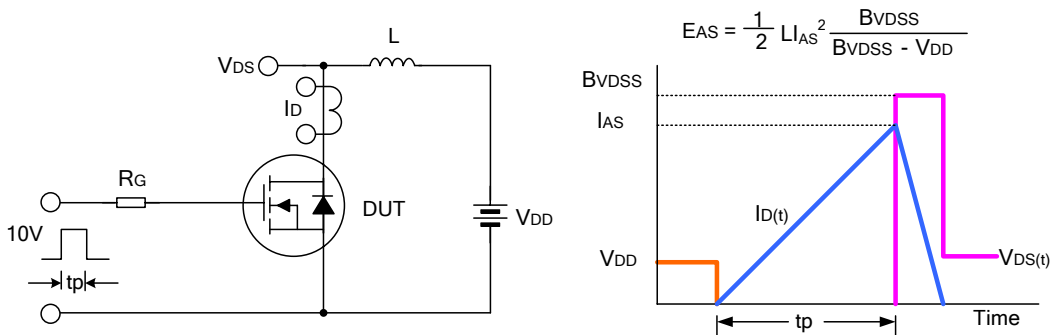
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



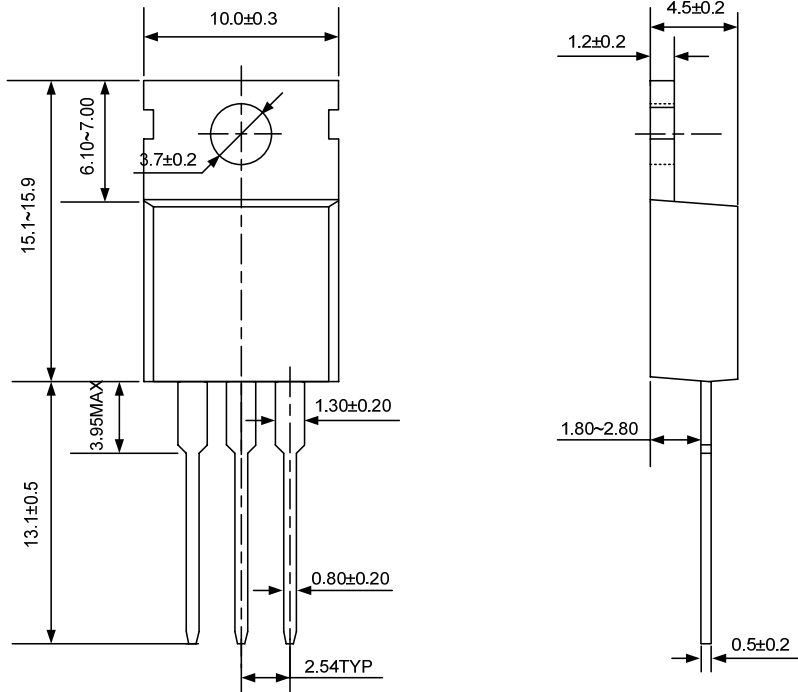
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

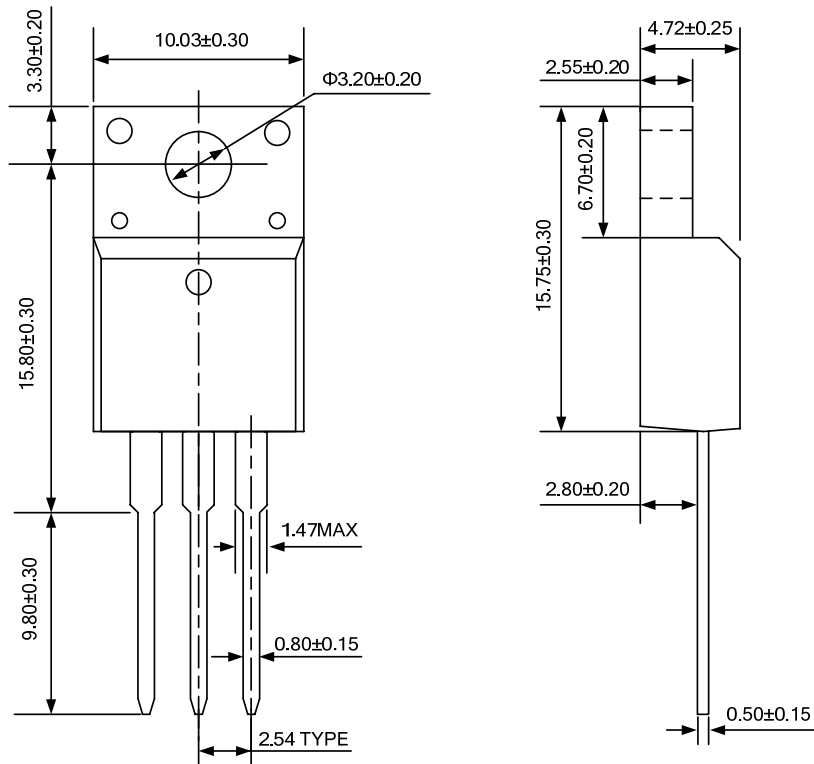
TO-220-3L

UNIT: mm



TO-220F-3L

UNIT: mm







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## ATTACHMENT

### Revision History

Date	REV	Description	Page
2010.12.13	1.0	Original	
2011.02.15	1.1	Modify "ABSOLUTE MAXIMUM RATINGS" and "ELECTRICAL CHARACTERISTICS"	